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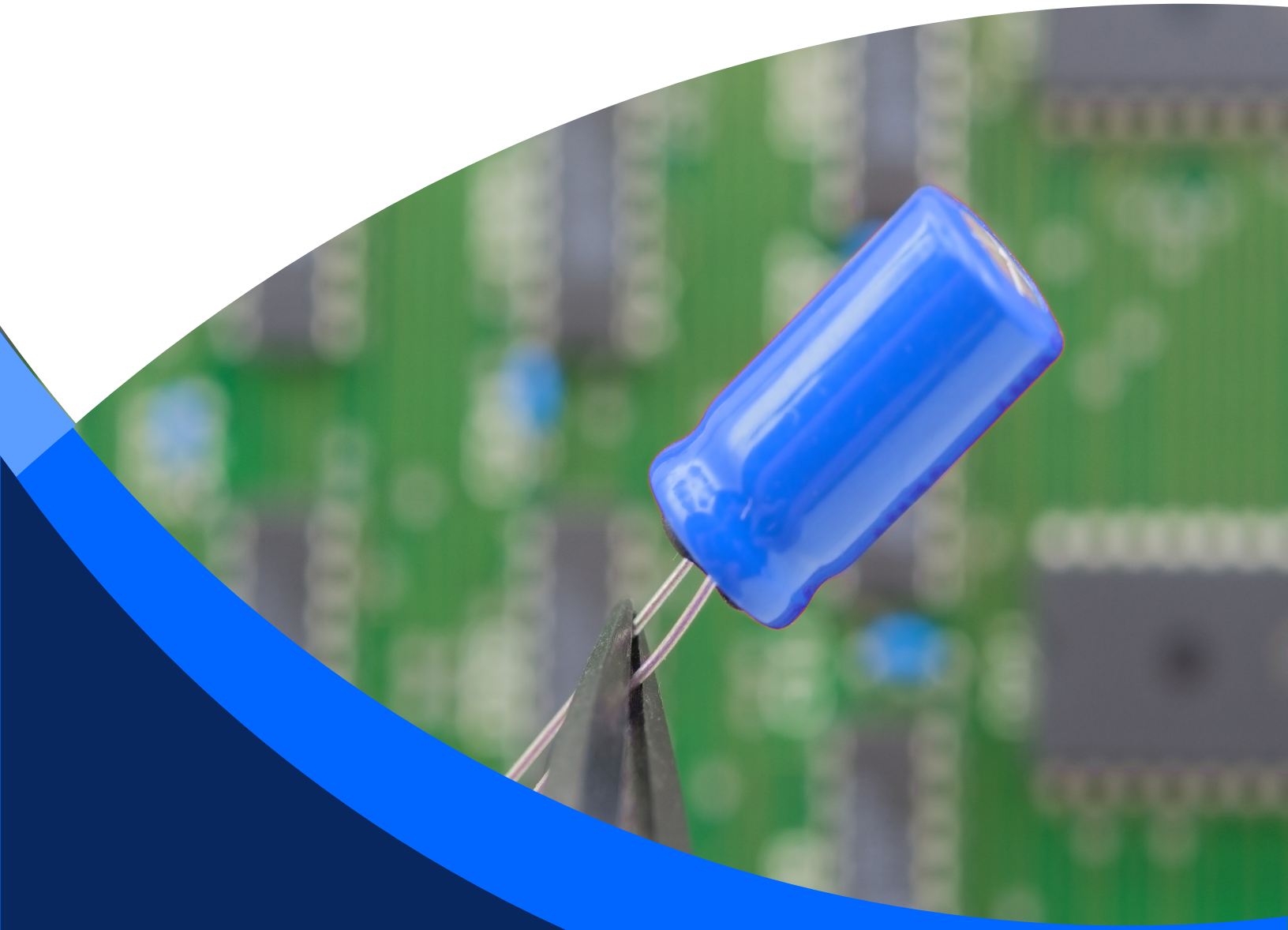

Supercapacitors Balancing Basics and Techniques

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Introduction

The rated voltage of supercapacitor cells is typically around 2.7 V. This is significantly lower than the rated voltage of traditional capacitors, such as ceramic or electrolytic types. As a result, it is often necessary to connect multiple supercapacitors in series to support the higher voltages required in electric vehicles (EVs), uninterruptible power supplies (UPS), voltage stabilization circuits, high-energy pulsed systems, memory backup applications, and other high-power systems. However, utilizing a series connection of supercapacitors reduces the total capacitance of the module, potentially decreasing it below the minimum design requirement. Although, this issue can easily be rectified by adding more strings of supercapacitors in parallel to increase equivalent capacitance, a major challenge that engineers face when designing such systems is maintaining a balanced voltage across all supercapacitors throughout the different operation phases. This brief will explore some of the basic techniques employed to avoid overvoltage conditions by balancing the voltages across a stack of series-connected supercapacitors.

Why Balancing Supercapacitors Is Important

Balancing series-connected supercapacitors is critical to avoid overcharging the cells, which could partially or fully damage them by breaking down the insulating dielectric or degrading the electrolyte solution. The purpose of the balancing circuit is to maintain an equal voltage across each of the cells. Otherwise, accidentally driving a cell beyond its' rated voltage could negatively impact the operational lifetime of the entire module. In addition, the utilization of a balancing circuit extends the operational lifetime by ensuring that each cell is operated below its rated voltage. This is typically known as voltage derating, please review Abracon Supercapacitor Lifetime Explained for more details.

Moreover, another critical issue balancing addresses is reverse biasing supercapacitors. This can happen during discharging phase where imbalanced capacitors are discharged to zero or low voltage. In this case, the external load might force a reverse polarity across one or more supercapacitors in the stack, leading to accelerated, often permanent damage.

What Causes Voltage Imbalance?

The physical tolerances of manufacturing processes and materials often lead to variations in the characteristics of different supercapacitor cells, even those produced within the same batch. These variations typically appear as differences in capacitance, ESR, and insulation resistance, which are the main contributors to voltage imbalances.

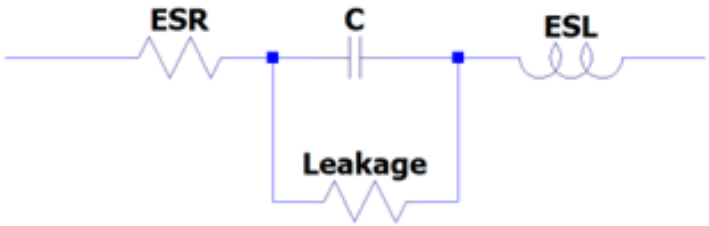

Figure 1: Supercapacitor equivalent circuit model

The dominant cause of voltage imbalance depends on the phase of the power cycle. At the start of the charging process, the imbalance is primarily caused by differences in capacitance. For example, supercapacitors commonly have tolerances of either -10/+30% or ±20%. This means that two cells can differ by as much as ±40% in capacitance. As will be explored in the next section, this difference can lead to a significant imbalance between the cells.

Once the cells begin idling after charging, voltage imbalance may gradually occur due to differences in insulation resistance, which in turn causes differences in leakage current. This imbalance, if left unaddressed for extended timeframe, could drive some cells beyond their rated voltages. Balancing ensures that leakage current from one cell does not cause an overvoltage condition in another.

It is worth noting that two components contribute to leakage current. The first arises from the exponential characteristic of the charging process, where time (t) must approach infinity for the charging current to reach zero; therefore, a small charging current continues to flow indefinitely. The second is due to the finite resistance of the dielectric insulator, which allows some current to leak between the electrodes of the supercapacitor.

Differences in ESR also result in voltage imbalance. However, the effect is typically negligible, as it is proportional to the charging current and the ESR of the cell. Assuming two cells with identical properties except for ESR, some imbalance will occur at the start of the charging process. However, the voltages across both cells will eventually equalize. Imbalance due to ESR becomes more apparent during discharge cycles, as it is also proportional to the discharge current. Voltage imbalance is also affected by other factors such as aging, environmental conditions, and the frequency of power cycling. All these have direct effects on capacitance, leakage, and ESR over time.

Quantifying the Steady-State Imbalance in the Series Stack of Supercapacitors

Let’s explore an example of calculating the voltage imbalance for the xth capacitor, Cx. Assuming a stack of n supercapacitors connected in series with zero initial charges and a voltage VS connected as follows:

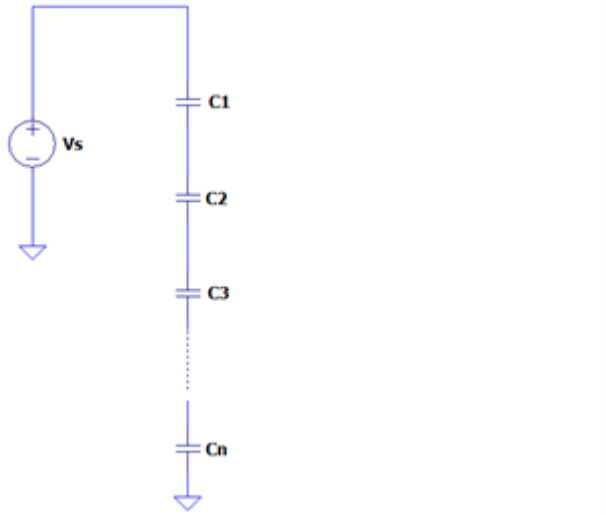

Figure 2: A series connection of n supercapacitors

As outlined earlier, voltage imbalance is caused by one of the following:

1. Voltage imbalance due to differences in capacitance:

The final voltage imbalance across the x^{th} capacitor (ΔV_{cx}) can be calculated as:

$$V_{Cx} = Vs * \frac{Ceq}{C_x} \quad (1)$$

$$\Delta V_{Cx(cap.)} = Vs * \frac{Ceq}{C_x} - (\frac{Vs}{n}) \quad (2)$$

2. Voltage imbalance due to differences in leakage resistance:

$$V_{Cx} = \frac{Vs * R_{xLeak}}{\sum_{j=1}^{n} R_{jLeak}} \quad (3)$$

$$\Delta V_{Cx(Leakage)} = V_{Cx} - (\frac{Vs}{n}) = \frac{Vs * R_{xLeak}}{\sum_{j=1}^{n} R_{jLeak}} - \frac{Vs}{n} \quad (4)$$

3. Voltage imbalance due to differences in ESR:

$$\Delta V_{Cx(ESR)} = \frac{Vs * ESR_X}{\sum_{j=1}^{n} ESR_j} \exp(\frac{-t}{\tau}) \quad (5)$$

Please refer to the Appendix section for more information about these equations and definitions of terms.

It should be noted that as time passes, imbalance due to differences in ESR exponentially decreases. Eventually, all capacitors will be balanced, assuming all other traits are exactly matched (capacitance and insulation resistance). However, voltage imbalance is the cumulative effect of all three parameters outlined above. The good news is that when designing a balancing circuit, there is no need to consider differences in capacitance, ESR, and leakage individually. All balancing techniques will attempt to balance the voltages across the cells regardless of the source of imbalance.

Common Balancing Techniques:

There are multiple methods that could be used to balance the voltage across a supercapacitor string.

Key considerations when selecting a balancing method include:

- Speed: How long it takes to bring unbalanced set of capacitors to a balanced state.
- Efficiency: How much power is consumed by the balancing circuitry during balancing or idling phases.
- Components count: Affects the cost of the solution and is limited by the available space.

Method 1: Passive Balancing Using Resistors (Voltage Divider):

This scheme employs a resistive voltage divider to balance series-connected stacks of supercapacitors. Each cell is connected in parallel to a resistor with a voltage source (Vs) powering the network as shown in Figure 3 below:

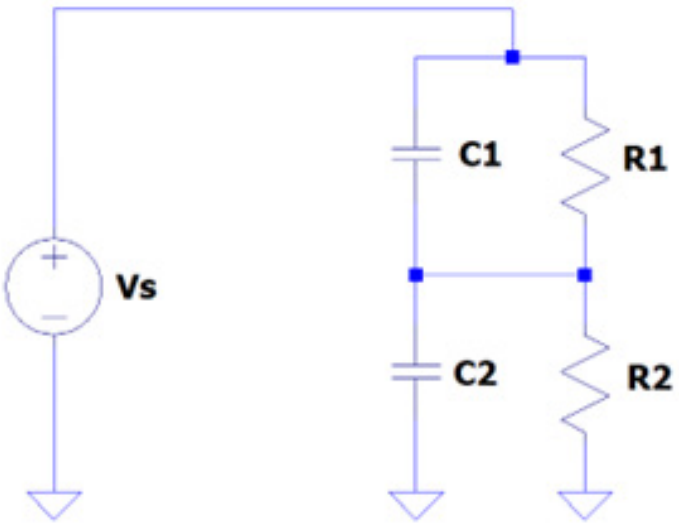

Figure 3: Passive voltage divider balancing circuit

Using a resistive voltage divider, we can easily set the midpoint voltage at the desired level. By selecting resistors of the same values, equal voltages can be achieved across both cells. In the case of an imbalance, the resistors network automatically discharges the extra voltage of the overcharged capacitor, while charging the other, until both capacitors have the same voltage.

A starting design point for the values of R1 and R2 can be chosen and set through the 10% rule-of thumb. It is a general rule that the load resistance (capacitors in this case) should be at least 10x higher than the resistors to avoid causing a voltage drop on the resistor. However, it's not a hard rule and intended as a reference:

$$R_{Balance} = 0.1 * \frac{V_{rated}}{I_{Leakage}} \quad (6)$$

Then, to calculate the time needed to get up to 98% of the required voltage across the SC:

$$t_{Balance} = ln(100\%/(100\% - 98\%)) * (R_{th} * C) \quad (7)$$

Where:

Rth: Thevenin equivalent resistance across the capacitor being charged.

The resistor values must be selected such that the trade-off between efficiency and balancing speed meets the design requirement. As Equations (6) and (7) show, choosing resistor values on the lower end leads to faster balancing speeds. However, this comes at the cost of lower efficiency due to the continuous heat losses in the resistors which are driven by the continuous current from the voltage source and the leakage currents from the capacitors. On the other hand, picking higher resistors values will lead to better efficiency due to the decreased current draw. However, balancing and charging times will be longer. For example, reducing resistors' values by 40% leads to a 40% faster balancing speed. However, efficiency decreases by a factor of [100%/(100%-40%)].

A simple, cost-effective solution can be realized using this technique. However, it is important to note that balancing performance is also affected by resistors' tolerances and variation over temperature. Additionally, this solution might not be suitable for applications with frequent cycling due to the slow balancing speed.

Method 2: Using Zener Diodes:

Zener diodes are connected in parallel with each capacitor, as shown in the Figure 4. These diodes are designed to conduct current in the reverse direction whenever the voltage across them exceeds the reverse breakdown voltage (also known as the Zener voltage). When the voltage across a capacitor exceeds the Zener voltage, the corresponding diode begins to conduct, allowing current to flow and charge the other capacitors while reducing the voltage of the overcharged one.

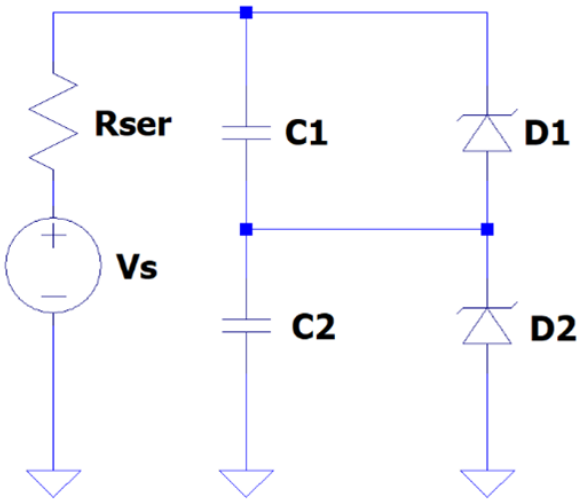

Figure 4: Active balancing using Zener diodes

Key considerations when selecting Zener diode method induce:

• Zener Voltage (Vz) (also known as reverse breakdown voltage): This is essential to the operation of the circuitry. This value must be equal or less the max voltage rating of the supercapacitors. Otherwise, they will not engage when an overvoltage occurs. Also, it is critical to know that Zener diode's tolerance can be up to ±10%. During steady state, the diodes keep the voltages across the supercapacitors at Vz.

• Max reverse current rating.

• Voltage-Temperature coefficient: Zener voltage changes with temperature. It is important to consider given that diodes dissipate power as heat.

Here are some of the advantages of using diode balancing:

• Low cost and simple designs

• Faster balancing speeds than resistive voltage divider. Diodes tend to consume more power than resistive voltage dividers during balancing. However, they are more efficient while idling as the currents through the diodes are limited by a series resistor as shown in Figure 4.

• Automated, no controllers are needed

Method 3: Active Balancing Using MOSFETs

Active balancing using MOSFETs is another method used to balance the voltages of multiple series-connected supercapacitors. The MOSFETs are connected in parallel to the capacitors as shown in Figure 5.

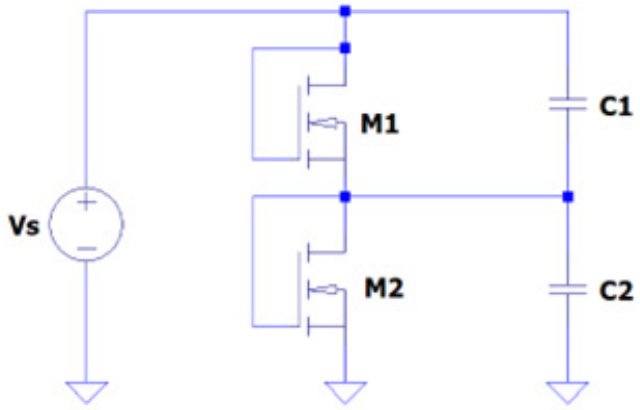

Figure 5: Active Balancing using MOSFETs

In this configuration, the enhancement mode n-type MOSFETs act as voltage-controlled resistors to recharge undercharged capacitors which reduces the voltage across overcharged capacitors at the same time.

A MOSFET will start conducting when the gate-to-source voltage (Vgs) exceeds the threshold voltage (Vth) of the transistor. Since the gate is connected to the drain, as shown in Figure 5, Vgs is equal to drain-to-source voltage (Vds) which is same as the voltage across the supercapacitor. Therefore, the MOSFET starts conducting current whenever the voltage across the parallel supercapacitor exceeds the threshold voltage (Vth).

To explain the process, let C1 and C2 be two imbalanced capacitors due to leakage or capacitance mismatch. Assuming C2 has larger leakage, without using any balancing techniques, the leakage current from C2 will increase the voltage across C1 (Vc1) until it exceeds its rated voltage (theoretically, the max it will reach is the source voltage Vs of M1).

In this case Vc1 is larger than Vc2. By introducing balancing MOSFETs as shown in Figure 5.

$$Vgs1 = Vds1 = Vc1 \qquad (8)$$

Where:
Vc1= is the voltage across the first capacitor.

Also, notice how this configuration forces Vds>=Vgs-Vth. This guarantees that the MOSFET is always operating in the saturation region whenever the voltage across the capacitor (Vc1 in this case) is above the threshold voltage. Hence, the drain current becomes:

$$Id1 = 0.5\ K\ (Vc1\ - Vth)\text{^}2 \qquad (9)$$

Where:
K: gain factor, usually constant and depends on the geometry/materials of the MOSFET.

As a result, the current through the MOSFET M1 is directly proportional to the first capacitor's voltage (Vc1). Next, as MOSFET M1 starts conducting more current, the voltage across it starts dropping which simultaneously increases the voltage at midpoint (Vc2). Vc2 continues rising until it reaches the threshold voltage (Vth2) of the second MOSFET M2 and turns it on, allowing it to conduct current, which limits the voltage across it to that level. M2 voltage cannot exceed this voltage limit since the configuration would force it to turn on, bringing the voltage across it down. So, in summary, we obtain an automated pendulum-like balancing effect where if imbalance occurs, the large voltage across one MOSFET forces it on, driving the voltage across it down while increasing the voltage across the other one, until both voltages are equal.

The following must be considered when selecting a MOSFET:

• The threshold Voltage (Vth) must be of a well-defined value (all MOSFETs must have equal threshold values) and should be equal or less than the rated voltage of the supercapacitors. Otherwise, the MOSFETs will never turn on. Note that the MOSFETs keep the balanced voltage at Vth during steady state.
• Max drain-to-source voltage (Vds) must be higher than the source voltage.
• Threshold Temperature Coefficient: Threshold voltage (Vgs-th) temperature dependance must be considered since MOSFETs dissipate power as heat.

Method 4: Active Balancing Using Op-amps:

This technique uses an operational amplifier (op-amp) to balance the voltage. The op-amp is configured as a voltage follower circuit in conjunction with a resistive voltage divider. The voltage divider, consisting of R1 and R2, sets the reference voltage (Vref) for the op-amp. The op-amp acts as a unity-gain buffer driving its output voltage to match Vref, which also sets the midpoint voltage between the two capacitors. Resistor R3 is used to limit the output current of the op-amp and to improve the stability of the feedback loop.

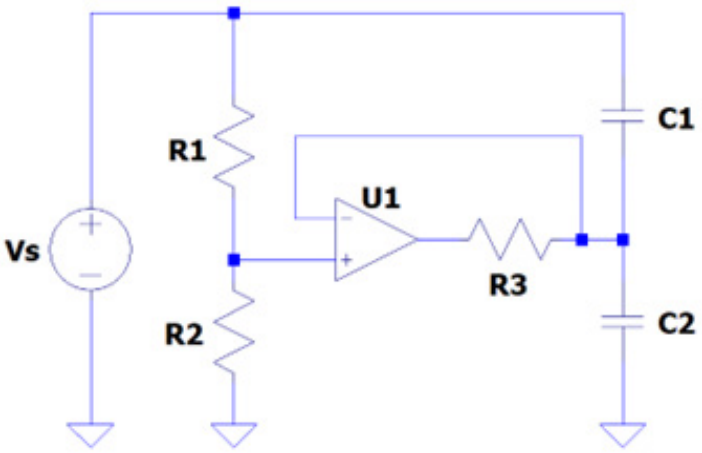

Figure 6: Active balancing using Op-amp

The main advantage of this method is its relatively fast balancing speed, which makes it more suitable for applications where frequent discharge occurs. However, this comes at the cost of higher power dissipation during balancing and an increased component count.

The op-amp is powered by the independent source voltage (Vs). No dual supply is needed in this case since the reference voltage used to set balancing point is always positive. The efficiency and balancing speed of this method depends on the characteristics of the op-amp like (quiescent power, max output current, max supply current ...etc) and the voltage divider resistors values. The designer can control the balancing speed and output current through the series output resistor R3. However, quantifying the trade-off between efficiency and speed needs more analysis of the op-amp characteristics.

Other Methods:

In addition to the techniques mentioned above, there are other approaches to address supercapacitor balancing including Bi-directional Buck-boosts DC-DC converters, specialized ICs LTC3350, TL431, DC1887A, BQ33100...etc. These solutions are available in fully integrated modules or can be implemented discretely, giving more flexibility to the design process.

Conclusion

Balancing supercapacitors is a preventive measure that helps protect against potential field failures due to overvoltage or reverse biasing. It also extends the operational lifetime by keeping the capacitor voltage below its rated value.

Imbalance occurs due to differences in capacitance, insulation resistance, and ESR. Choosing capacitors produced from the same batch helps minimize mismatches and large voltage imbalances. However, imbalance is also affected by factors such as aging and environmental conditions.

There are multiple balancing techniques that involve the use of passive components, active components, integrated circuits (ICs), or complete modules. The trade-offs between these methods include balancing speed—which depends on how much current each method can handle—and efficiency, which is determined by the power consumed by additional components. Another important consideration is the available PCB real estate and overall cost. Abracon offers a wide range of supercapacitors in various forms and sizes, tailored to suit diverse requirements. Check Abracon Supercapacitors for more information.

Appendix:

1. Voltage imbalance due to differences in capacitance:

$$V_{Cx} = Vs * \frac{Ceq}{C_x}$$

$$\Delta V_{Cx(cap.)} = V_{Cx} - (\frac{Vs}{n})$$

Where:

V_{CX} : Voltage across the x^{th} capacitor

V_s: Source voltage

C_{eq}: The total equivalent capacitance of the string

C_x: Capacitance of the x^{th} capacitor

n : Number of capacitors in the string

$\Delta V_{(Cx(cap.))}$: Voltage imbalance (or deviation from the ideal voltage) due to difference in capacitance

2. Voltage imbalance due to differences in leakage resistance:

$$V_{Cx} = \frac{Vs * R_{xLeak}}{\sum_{j=1}^{n} R_{jLeak}}$$

Where:

Rx_{Leak}: Leakage resistance of the x^{th} capacitor

Rj_{Leak} :Leakage resistance of the j^{th} capacitor

$$\Delta V_{Cx(Leakage)} = V_{Cx} - (\frac{Vs}{n}) = \frac{Vs * R_{xLeak}}{\sum_{j=1}^{n} R_{jLeak}} - \frac{Vs}{n}$$

3. Voltage imbalance due to differences in ESR:

$$\Delta V_{Cx(ESR)} = \frac{Vs * ESR_X}{\sum_{j=1}^{n} ESR_j} \exp(\frac{-t}{\tau})$$

Where:

$\Delta V_{Cx(ESR)}$:Voltage imbalance caused by differences in ESR
ESR_X: ESR of the xth capacitor
ESR_j: ESR of the jth capacitor
τ: time constant
t : time

In cases where constant current is used to charge and discharge the capacitors, the constant current (In) that must flow in or out of the nth capacitor to balance the voltage with a specified period (Δt) becomes:

$$In = Cn * \frac{\Delta Vn}{\Delta t}$$

Where:

Δ_t: time it takes to balance the voltage (Sec.)
Δ_{Vn}: voltage imbalance of the nth capacitor