ABRACON
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Second Generation ClearClock™ Third-Overtone Crystal Oscillators

Improving low RMS phase jitter performance in miniature packages.

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Introduction

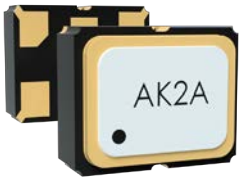
Small form factors allow system designers to keep their products condensed and compact, but the reduced size comes at a performance cost compared to larger versions of the same components. For high-speed computations and operations, many applications require extremely low jitter from the reference clock. System designers evaluate the trade-offs and alternatives to search for the best combination of size and rms phase jitter performance. Some applications that use such low jitter technology include optical modules, cloud computing, networking, data storage, PCIe-5/6, 100G/200G/400G/800G Ethernet and other RF applications.

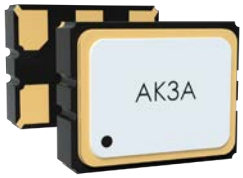
Generation-I Differential Clock Solutions

In 2019, Abracon released its first generation AK2 and AX3 series as part of the ClearClock™ family of ultra-low jitter quartz crystal oscillators. These third-overtone solutions were created to keep up with the demand for 100 to 200 MHz clocking solutions in small package sizes; particularly PCI Express, optical transceivers, data storage, and networking designs. Abracon ClearClock™ solutions are offered in LVPECL, LVDS, and HCSL outputs across this frequency range.

Generation-II Differential Clock Solutions

With the development of new oscillator IC technology, Abracon released the next generation of ClearClock™ oscillators: the AK2A and AK3A series. Matching the smaller footprints of the AK2 (2.5 x 2.0 mm) and AX3 (3.2 x 2.5 mm) respectively, the AK2A and AK3A series offer improved rms phase jitter performance without sacrificing their compact form factor. For example, at 156.25 MHz carrier frequency, the AK3A offers a typical RMS jitter of 72 fs for its HCSL output, improved from the AX3's typical 113 fs RMS jitter performance over the 12kHz to 20MHz BW from the carrier.





Taking a closer look at this example, the AK3A has a 3.2 x 2.5 mm footprint and delivers 72 fs typical RMS jitter over an offset bandwidth of 12 kHz – 20 MHz (referenced from the carrier frequency), with a maximum specification limit of 100 fs. RMS phase jitter is a time domain parameter that is derived from the phase noise (frequency domain) measurement. Figures 1 and 2 show the phase noise plots of the corresponding AK3A and AX3 part numbers (AK3AHAQ1-156.25MHZ and AX3HAQ1-156.25MHZ). Both parts are operated at 3.3V with a 156.25 MHz differential HCSL output. Note that at frequency offsets starting at 100kHz, the AK3A has a lower phase noise floor than the AX3, reaching -161 dBc/Hz at a 20MHz offset.

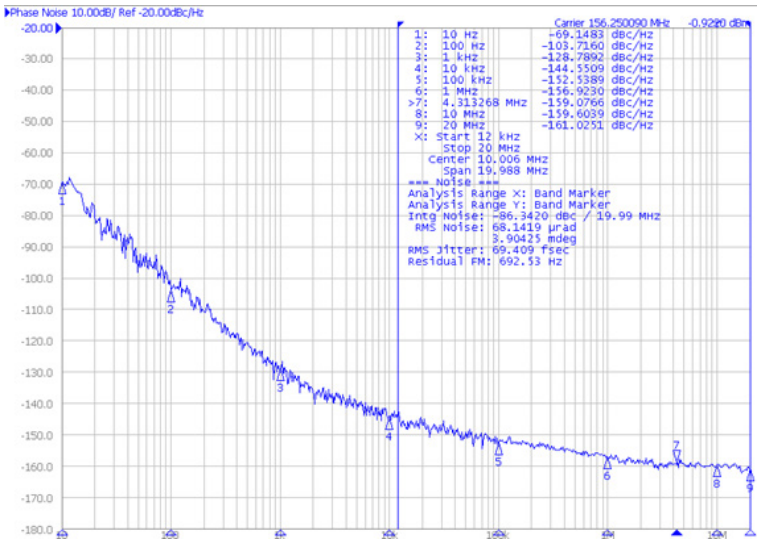


Figure 1: AK3A Phase Noise Plot (HCSL, 3.3V)

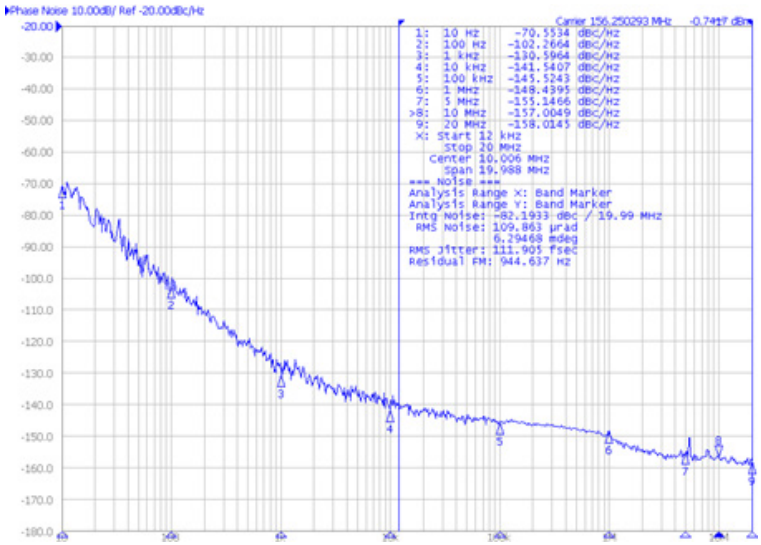


Figure 2: AX3 Phase Noise Plot (HCSL, 3.3V)

AK3A vs AX3 RMS Phase Jitter (HCSL, 3.3V, 156.25MHz, Typical)	
AK3A (Gen II)	AX3 (Gen I)
69.4 fs	111.9 fs

Table 1: AK3A vs AX3 RMS Phase Jitter

The difference in phase noise is more pronounced in Figure 3, which places both phase noise graphs on the same plot. The AK3A's lower phase noise plot results in the improvement in RMS phase jitter (12kHz - 20MHz). AK3A solutions are ideally suited for end-applications requiring 100fs maximum rms jitter performance.

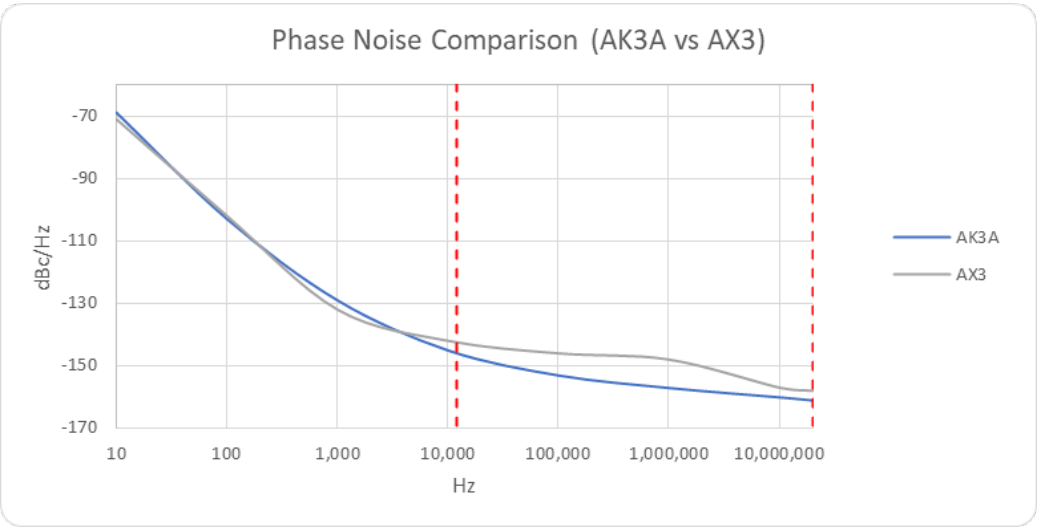


Figure 3: AK3A vs AX3 Phase Noise Comparison

Abracon's ClearClock™ oscillator series are available in multiple output logic types, including HCSL, LVDS, and LVPECL. The AK3A example above depicts the performance with HCSL output.

Similarly, significant rms jitter improvement is achieved with the AK2A series compared to first-generation counterpart [AK2]. Figures 4 and 5 show the differences between the AK2A and AK2 series at 100 MHz (LVDS output).

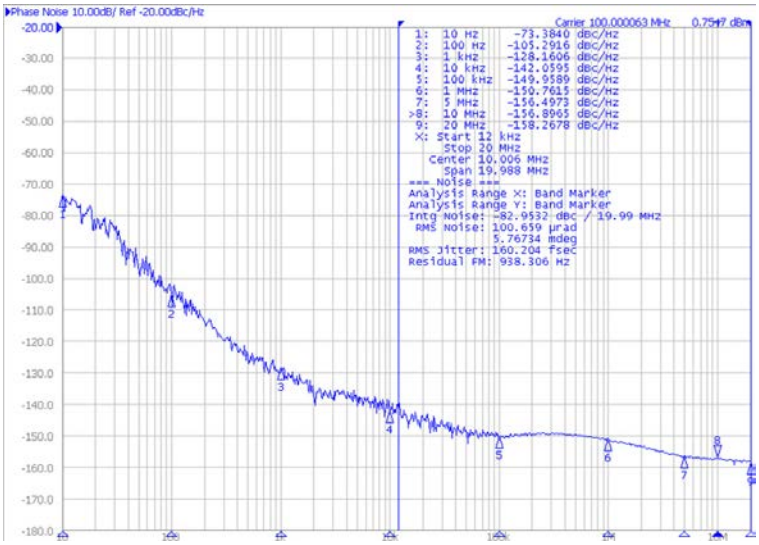


Figure 4: AK2A Phase Noise Plot (LVDS, 3.3V)

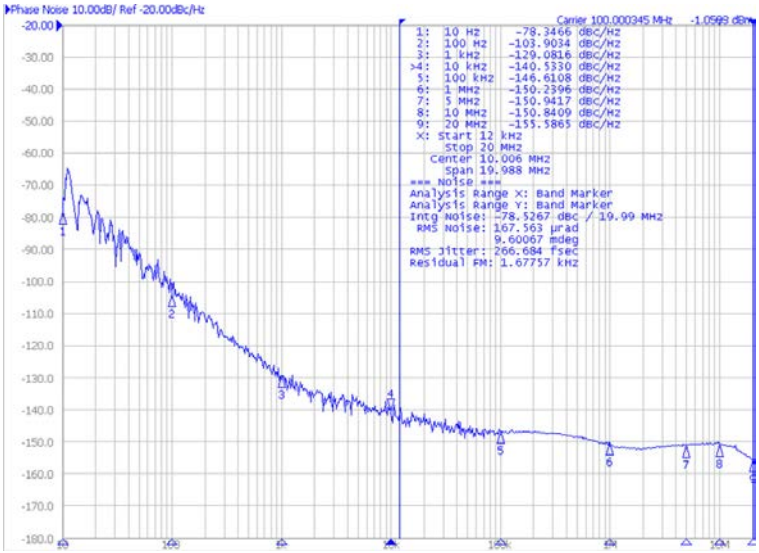


Figure 5: AK2 Phase Noise Plot (LVDS, 3.3V)

AK2A vs AK2 RMS Phase Jitter (LVDS, 3.3V, 100.000MHz, Typical)	
AK2A (Gen II)	AK2 (Gen I)
160.2 fs	266.7 fs

Table 2: AK2A vs AK2 RMS Phase Jitter

Similar to AK3A, the improvement in phase noise performance is more evident when observing the differences in measurement floors at a 12 kHz to 20 MHz offset from the carrier frequency, as shown in Figure 6.

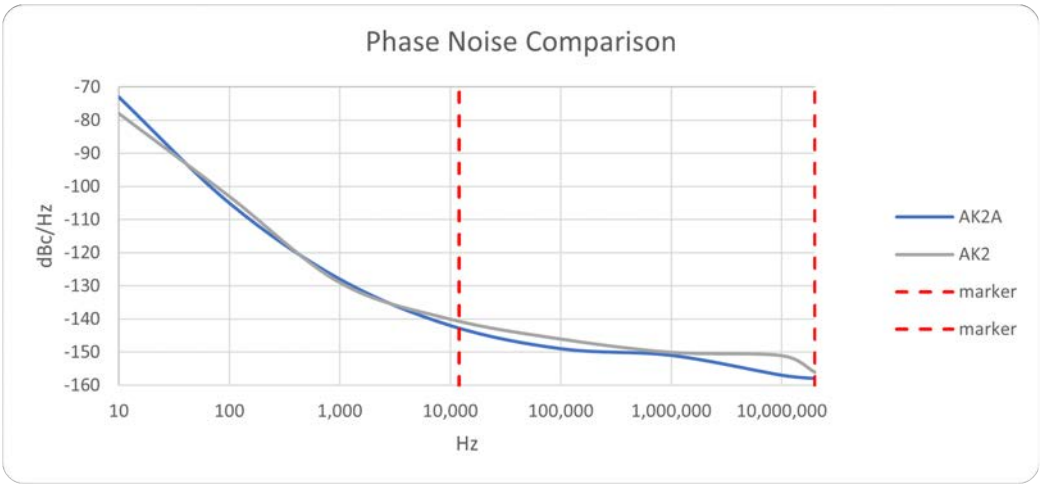


Figure 6: AK2A vs AK2 Phase Noise Comparison

Specific RMS phase jitter performance for all parts discussed above is outlined in Tables 3 and 4. It should be noted that the phase noise performance will differ with carrier frequency, supply voltage, package size, and output logic. The percentage improvement in tables 3 and 4 clearly depict the significant improvement in rms jitter performance, as the ClearClock™ series evolved from generation-I to generation-II.

AK3A vs AX3 — RMS Jitter Comparison			
	AK3A (Gen II)	AX3 (Gen I)	% Reduced
HCSL, 156.250 MHz	69 ps	112 ps	-38%
LVDS, 100 MHz	160 ps	268 ps	-40%
LVDS, 156.25MHz	81 ps	119 ps	-32%

Table 3: AK3A vs AX3 RMS Phase Jitter (Vdd = 3.3V, Typical)

AK2A vs AK2 — RMS Jitter Comparison			
	AK2A (Gen II)	AK2 (Gen I)	% Reduced
HCSL, 100 MHz	152 ps	181 ps	-16%
LVDS, 100 MHz	160 ps	267 ps	-40%
LVDS, 156.25MHz	83 ps	122 ps	-32%

Table 4: AK2A vs AK2 RMS Phase Jitter (Vdd = 3.3V, Typical)

Trade-offs

The AK2A and AK3A utilize the next-gen oscillator ASIC, ensuring ultra-low rms jitter performance at a slight cost to power consumption. With the maximum current consumption increasing from 50 mA (Gen I) to 60 mA (Gen II), the second generation ClearClock™ oscillators are prime candidates for achieving ultra-low-rms-jitter while maintaining low power consumption.

Conclusion

System designers require cutting edge solutions that optimize the balance between size, power draw, and jitter performance. Abracon's ClearClock™ oscillator family provides an excellent combination of small form factor, low power consumption, and ultra-low rms jitter performance. Both Gen I [AK2 & AX3] and Gen II [AK2A & AK3A] products offer premium rms jitter performance; with Gen II ensuring 100fs maximum rms jitter at or above 156.25MHz carriers.