Understanding the basics of the Pierce oscillator

The designer's challenge is to optimize performance with the quartz crystal

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Today, the majority of electronic circuits (including microprocessors, microcontrollers, FPGAs, and CPLDs) are based on clocked logic, requiring a timing source. Depending on the frequency accuracy requirements, some employ oscillators while others use off-the-shelf quartz crystals in conjunction with the built-in oscillator circuit embedded in most microcontrollers and microprocessors.

Most if not all embedded solutions use the Pierce oscillator configuration, integrated as part of the SoC (system-on-chip). The obvious advantages include cost, size, and power compared to a standalone oscillator. The key limitation is the proper matching of the quartz crystal with the on-board Pierce oscillator.

Figure 1 outlines the oscillator block and the key components that influence the overall performance of the timing loop. Let the effective load capacitance, as seen by the crystal, be C_L. Then

$$C_L = \frac{(C_{IN} + C_1)(C_2 + C_{OUT})}{C_{IN} + C_1 + C_2 + C_{OUT}} + \text{Board Strays} \qquad (1)$$

For example, let $C_1 = C_2 = 27$ pF; $C_{IN} = 5.0$ pF and $C_{OUT} = 10.0$ pF and Board Strays = 0.50 pF. Then

$$C_L = \frac{(27 + 5)(27 + 10)}{5 + 27 + 27 + 10} + 0.50 = 17.65 \text{ pF}$$

Therefore specifying a crystal with 18.0 pF plating load capacitance would be the closest match for frequency accuracy. The selected capacitors primarily influence the overall oscillator loop capacitance, as seen by the crystal. This effective loop capacitance (C_L from Eq. 1) determines how far the oscillator loop is resonating, relative to the desired resonant frequency. However, the overall long-term performance of the oscillator loop is influenced by the following factors:

- The reactive impedance (Xc) of these loop capacitors.
- The inverter amplifier's transconductance (gm).
- The presence or absence of the current limiting resistor (Rs).
- The presence or absence of the automatic gain control (AGC) or automatic level control (ALC); with-in the integrated oscillator circuit.

These factors collectively set the boundary condition of the design. This boundary condition, commonly referred to as the safety factor (SF), is an important parameter to ensure that the product design has sufficient margin to accommodate part-to-part and lot-to-lot variations; as well as, eliminating product performance uncertainty in production volume.

Historically, design engineers have optimized their circuit performance via trial and error, at the expense of significant investment in time. Further, to properly determine the oscillator loop dynamics, the most accurate determination is made by breaking the oscillator loop and conducting key measurements using specialized equipment such as a current probe.

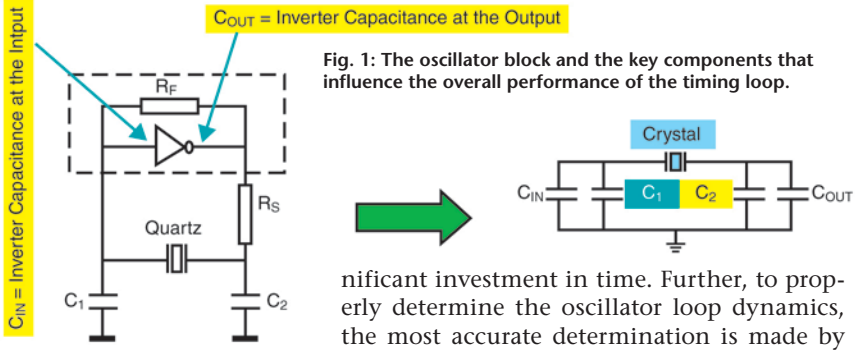

Fig. 1: The oscillator block and the key components that influence the overall performance of the timing loop.

Lastly, these measurements become increasingly sensitive if the timing loop is driven by a tuning-fork (32.768-kHz) crystal. These crystals are extremely sensitive to loading effects and to accurately determine the in-circuit behavior of these components, extreme care and accuracy is essential. For instance, Automotive, medical and consumer electronics solutions typically use tuning fork crystals for their real-time-clocking (RTC) needs. If the selected SOP has limited gain margin, there is a high probability that some percentage of these crystals will not properly start under adverse conditions, such as cold operating temperature (–40°C).

Another example would be a product designed to address the ZigBee related solutions, which typically has a hard boundary condition of ±40 ppm relative to the carrier, for proper operation. This ±40-ppm operational window actually needs to account for

- Quartz crystal set tolerance.
- Shift through reflow.
- Stability over temperature.
- Aging during product-life-cycle (such as 5 years).
- Frequency pushing and pulling.

If the oscillator loop is not optimized, most of the ±40 ppm can be potentially consumed by the set tolerance of the quartz crystal alone, thereby causing potential field failures.

These frequency domain failures could be primarily attributed to the oscillator frequency drifting over temperature or long-term aging, to the point that the oscillator loop is no longer within the allocated ±40-ppm operational window.

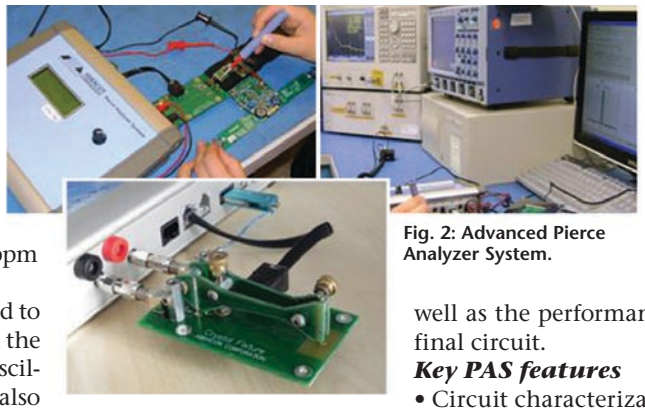

Fig. 2: Advanced Pierce Analyzer System.

Besides the issues related to oscillator-loop accuracy in the frequency domain, the oscillator-loop drive level must also be properly quantified to ensure acceptable product performance over temperature and time. For instance, a typical 24-MHz SMT quartz crystal has a drive level specification of 100 µW max. If the quartz crystal is consistently being driven at some multiple of this limit, such as 200 µW; it is possible that, over temperature or time, the oscillator circuit might start to resonate permanently or intermittently — at a spurious or overtone mode of the quartz crystal.

Although relatively low on the checklist of design engineers, the Pierce oscillator driven by an external resonator — such as a quartz crystal — can present a significant challenge during a typical product launch. Characterizing the oscillator loop during the design phase should be a priority to mitigate the risk during product launch as well as field returns down the road.

The Pierce Analyzer System

To overcome these challenges and provide an accurate assessment of the oscillator loop dynamics, Abracon's Advanced Engineering Team has developed a proprietary Pierce Analyzer System (PAS), designed to analyze both the standalone crystal, as well as the performance of that particular crystal in the final circuit.

Key PAS features

- Circuit characterization; provides best possible match between Quartz Crystal, oscillator loop and associated components.
- Eliminates probability of oscillator startup issues related to inadequate design or marginal component performance.
- Eliminates production launch issues related to crystal oscillator based timing circuit.
- Solves for design margin uncertainty.
- Provides customer's oscillator circuit overview in the form of a detailed report, which could be an ideal 3rd party assessment for the design history file or PPAP documentation. This report encompasses both the stand-alone crystal performance, as well as in-circuit behavior outlining safety factor as a function of crystal's ESR, etc.