

Jitter-Optimized, Miniature & High Frequency XO

The optimal convergence in small size and jitter performance

System designers face a fundamental challenge related to reference clock jitter due to an ever-increasing need for smaller form factors: As the size of the quartz crystal inside the reference oscillator is reduced, the ability to hold superior rms jitter performance becomes challenging. With the constant demand on both overall system size and functionality, designers are seeking reference clocks that meet the optimal convergence in small size and jitter performance.

PLL-based Solutions

From inception, Abracon has been keenly focused on consistently achieving this convergence and producing ultra-low rms jitter clocking solutions in miniature form factors. In 2018, Abracon launched two solutions under its ClearClock™ family, the AX5 and AX7 devices in 5x3.2mm and 5x7mm packages, respectively. These devices are based on sophisticated PLL technology, as shown in Figure 1, yielding superior rms jitter performance – typically better than 150fs over 12kHz to 20MHz from the carrier.

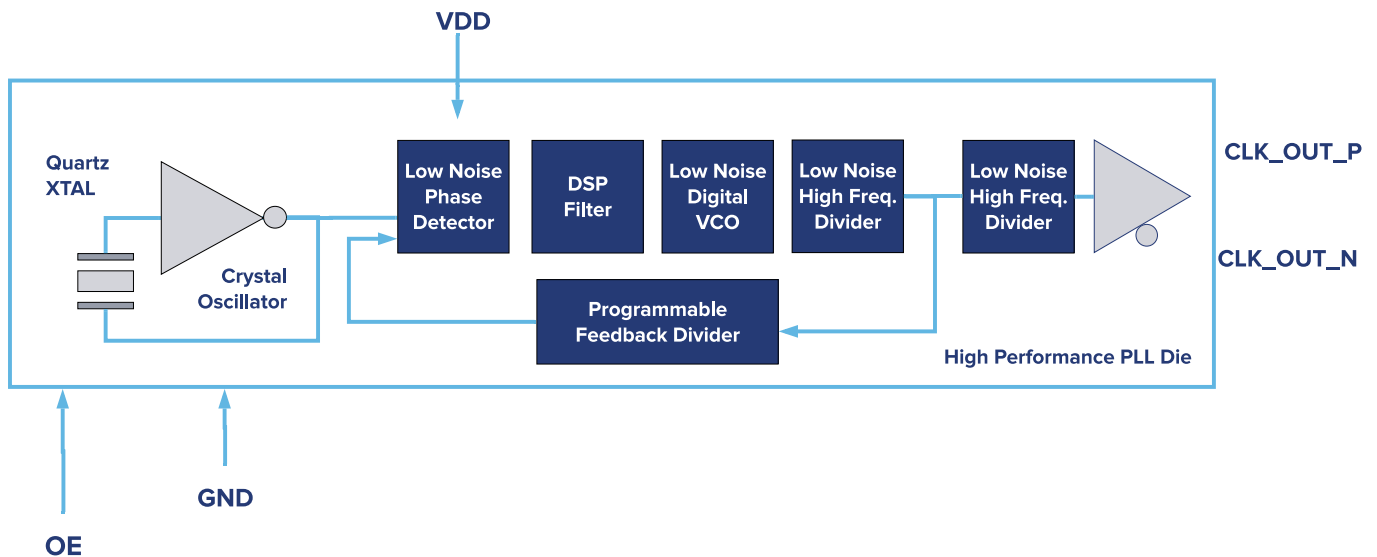


Figure 1: PLL-based AX5 and AX7 Series architecture

In the above PLL approach, techniques were employed to improve the limitation of the phase noise detector floor so that the phase noise slope has improved convergence – further away from the carrier. The AX5 and AX7 devices are optimized to service market needs between 50MHz and 2.1GHz carrier frequencies. These devices can be configured to any desired frequency between the previously specified range at Abracon’s production facility. With the ability to offer industry-leading upper frequency limit, AX5 and AX7 solutions are ideally suited for applications that require greater than 200MHz clocking reference.

Non-PLL-based Solution

However, Abracon further recognized an ever-increasing need for customers requiring 100MHz and 156.25MHz carrier frequencies in even smaller form factors than the AX5 and AX7 devices. These requirements are typically centric to the PCI Express (PCIe), optical transceiver, storage and networking customer base.

In response, Abracon developed a solution with superior jitter performance in a miniature package size. The company recently introduced the AX3 series of ultra-low-rms-jitter clocks in a 3.2x2.5x1.0 mm package. This family is available with LVPECL, LVDS or HCSL output configuration.

The AX3 devices can be biased at +1.8V, +2.5V or +3.3V with LVDS or HCSL outputs and at +2.5V and +3.3V with LVPECL output configuration. With a comprehensive understanding of market needs, Abracon has developed (12) unique carrier frequencies in the AX3 family of ultra-low-jitter clocks listed below:

100.00, 114.00, 114.285, 120.00, 122.88, 125.00, 135.00, 148.50, 150.00, 155.52, 156.25 and 200.00 MHz

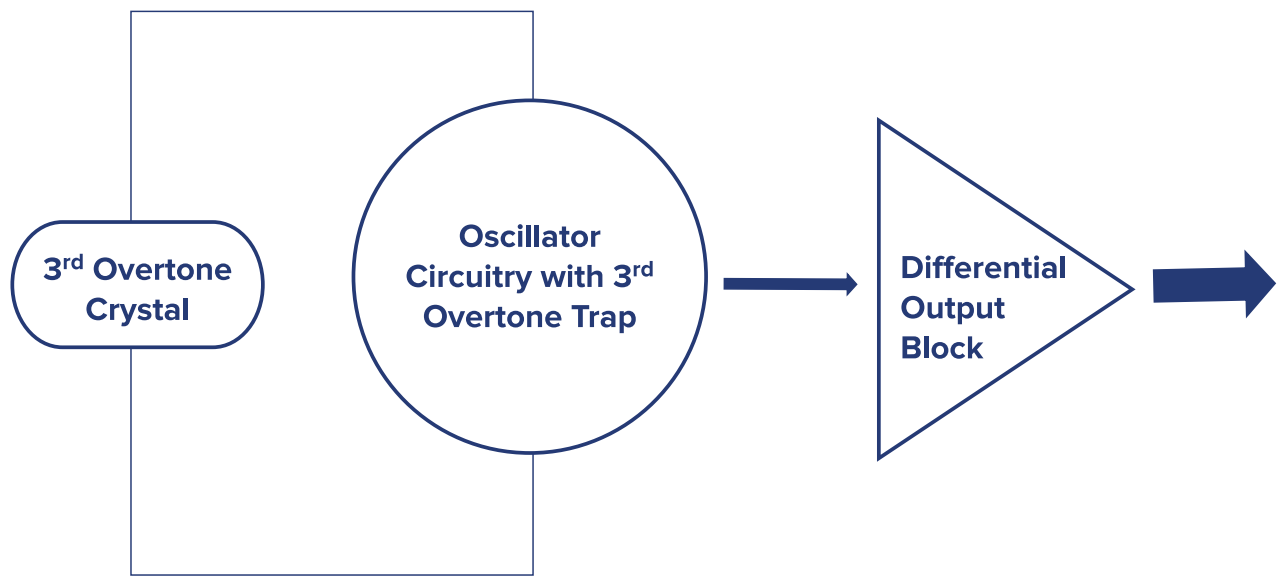


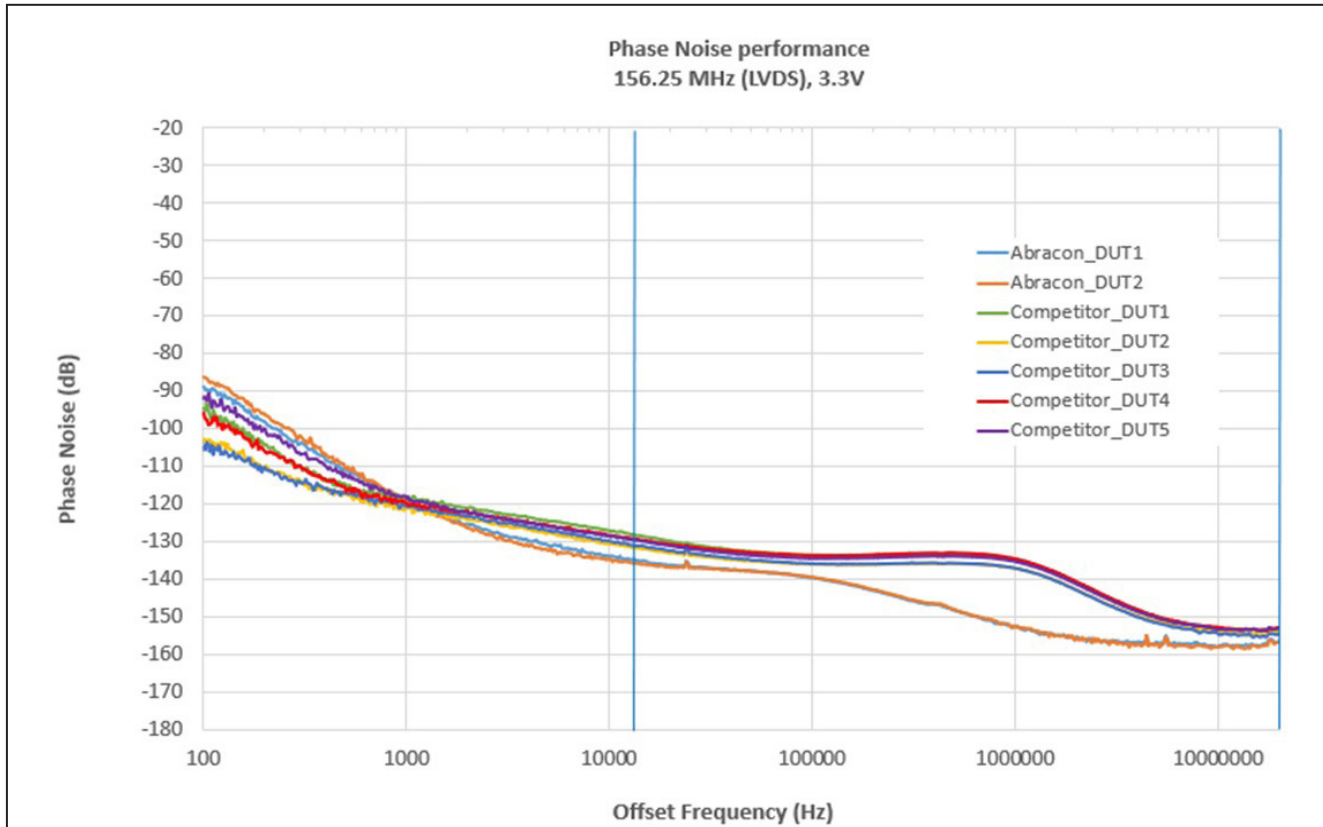
Figure 2: Non-PLL-based AX3 Series architecture

The secret of the AX3 performance lies in its simplicity. Careful design of the third overtone crystal blank, along with the proper trapping of the desired carrier signal, ensures an outstanding rms jitter performance at the carriers of interest.

As evident in Figure 2, the AX3 architecture does not employ a typical PLL approach, so there is no “up-conversion.” Simply speaking, there is no fractional or integer multiplication employed to the generated signal and therefore, the final output frequency has a one-to-one correlation to the resonant frequency of the third overtone quartz crystal. The absence of fractional multiplication simplifies the design and provides the best possible jitter in a miniature 3.2x2.5x1.0 mm package.

Abracon compared the performance of the AX3 family to the primary competitor’s solution in the same package size. As illustrated in Figure 3, the AX3 outperforms the primary competitor by an average of 68% for rms jitter performance at 156.25MHz carrier.

Abracon believes that the competitor’s solution is based on Inverted Mesa Crystal technology and does not employ the third overtone crystal architecture as the AX3 family. Further, the active circuitry inside the competitor’s device exhibits a threshold of approximately -135dBc/Hz between 10kHz to 1MHz offset from the carrier. This limitation contributes toward lesser rms jitter performance over the bandwidth of interest (12kHz to 20MHz).



Offset Frequency (Hz)	Abracon_156.25 MHz_3.3V		Competitor_156.25 MHz_3.3V		
	DUT 1 (dBc/Hz)	DUT 2 (dBc/Hz)	DUT 1 (dBc/Hz)	DUT 2 (dBc/Hz)	DUT 3 (dBc/Hz)
100	-88.76	-86.46	-94.80	-96.51	-92.41
1k	-118.69	-119.28	-118.30	-120.07	-119.13
10k	-134.05	-135.03	-127.28	-128.65	-128.63
100k	-139.60	-139.70	-133.86	-133.80	-134.49
1M	-152.76	-152.78	-135.21	-134.68	-135.29
5M	-156.81	-157.45	-150.24	-149.91	-150.20
10M	-158.06	-158.34	-153.01	-152.79	-153.29
20M	-156.55	-157.28	-153.39	-152.87	-153.00
RMS jitter (fs)	122.787	117.565	387.722	406.41	-380.116

Figure 3: Abracon AX3 Series Performance vs. Top Competitor

To ensure compliance to ± 50 ppm all-inclusive frequency stability over a 20-year product life, Abracon optimized the third overtone crystal and conditioned it to meet ± 15 ppm stability over -20°C to $+70^{\circ}\text{C}$ and ± 25 ppm stability over -40°C to $+85^{\circ}\text{C}$, as shown in Figure 4.

With set-tolerance, shift through reflow, frequency pulling and pushing and aging over a 20-year product life – this optimization ensures that the AX3 family of devices will remain well-within the desired ± 50 ppm all-inclusive boundary condition over the 20-year product life.

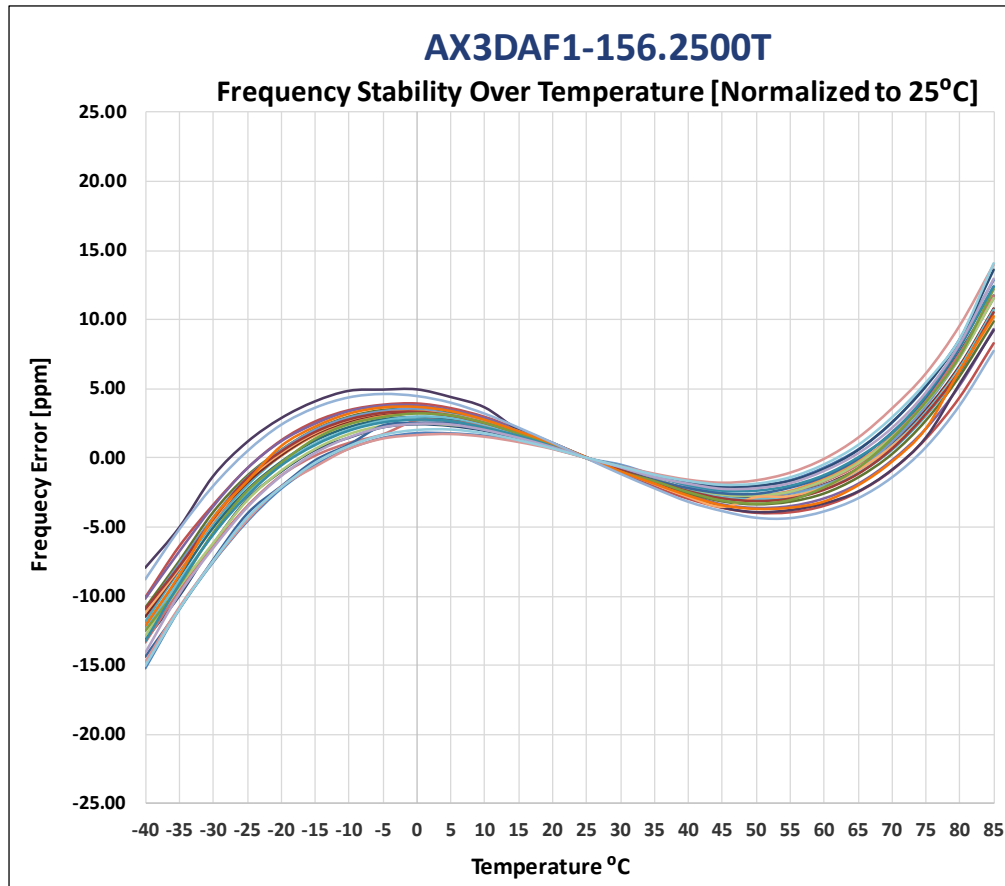


Figure 4: AX3 ± 15 ppm stability over -20°C to $+70^{\circ}\text{C}$ and ± 25 ppm stability over -40°C to $+85^{\circ}\text{C}$

System designers require innovative clocking solutions that meet size, performance and cost constraints. Abracon’s ClearClock™ family of devices provide the ideal convergence of small size and superior jitter performance. In particular, the AX3 family outperforms its competition at 100MHz and 156.25MHz carrier frequencies.

Lastly, to ensure quick availability for both the design community as well as mass production needs, Abracon’s AX3 clock oscillators at majority of the developed frequencies will be available through the company’s global distribution network starting in August 2019.

Author Information:

Syed Raza
 VP of Engineering
 Abracon, LLC.