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ClearClock for the Future of PCIe

ClearClock for PCIe 6.0 and Prior Revisions

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Introduction

Serial interfaces are moving into the realm of 32GT/s with PCI Express 5.0 hardware making its way to the market, but the widespread pursuit of machine learning and graphics intensive applications has pushed the Peripheral Component Interconnect Special Interest Group (PCI-SIG) to accelerate the publication of the PCIe 6.0 specification. PCI-SIG announced the PCIe 6.0 specification for a 2021 release [1]. As one of the industry leaders in timing, Abracon is meeting and exceeding the demands for the clock specifications of the future.

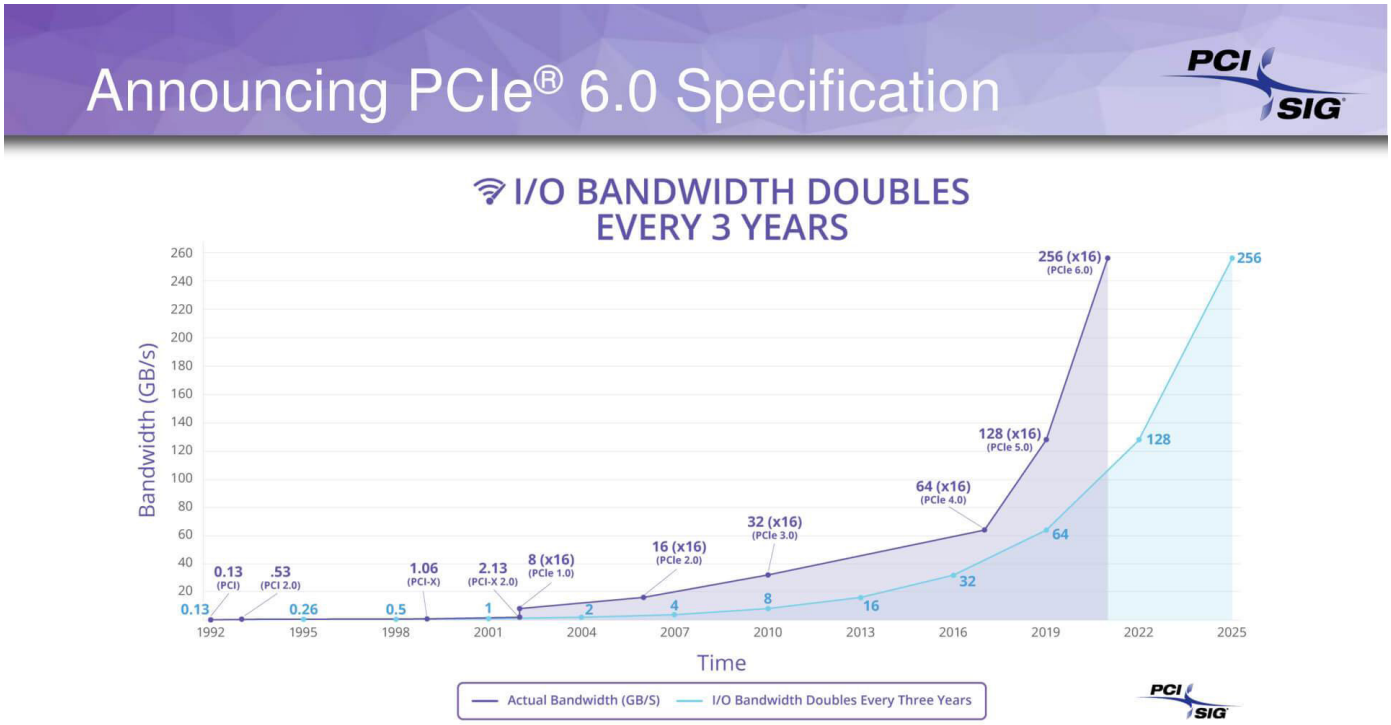

Figure 1: Generational Bandwidth Increases [1]

The Abracon ClearClock™ family's third-overtone quartz crystal oscillators are well equipped for PCIe 5.0 and are prepared for the challenges that are uniquely presented by the upcoming PCIe 6.0 release. The ClearClock™ [8] family of oscillators leads the industry in low power consumption while maintaining typical rms phase jitter as low as 70fs.

PCIe Progression

In 2003, the PCI Express standard was introduced to replace the parallel PCI bus. The current form factors target devices that range from IoT designs, handheld devices, data center applications, and automotive solutions. The standard is currently on the 5th Generation (Gen. 5.0) and is expected to move to the 6th generation (Gen. 6.0) in Q4 2021 (Figure 1).

The widespread adoption of PCIe is based on the demand for emerging markets, such as cloud computing, artificial intelligence and automotive, along with growing existing markets, such as enterprise servers, personal computing and IoT. These markets need a universal interface that has a focus on speed, cost, long-term compatibility and reliability, which PCIe gladly meets.

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PCIe Link Layer

PCIe is made up of abstraction layers similar to the network OSI stack, which entails the software, transaction, data link, logical PHY, electrical, and mechanical layers. This paper will focus on the electrical and physical layers since the reference clock performance primarily affects those two layers. The data link layer will be discussed for relevant application purposes and will provide background leading into Gen. 6.0 electrical specifications.

To better understand the background of PCIe and its purpose, it is important to understand how PCIe transmits and receives data. Transactions can take place on a variable number of lanes with up to 32 lanes, although most devices offer no more than a 16-lane interface (Figure 2). The latest Gen. 5.0 specification reaches 32Gb/s and the most prevalent PCIe devices rely on the 4th generation specification of 16Gb/s. The upcoming Gen. 6.0 specification will double the bandwidth from Gen. 5.0 and quadruple the bandwidth of Gen. 4.

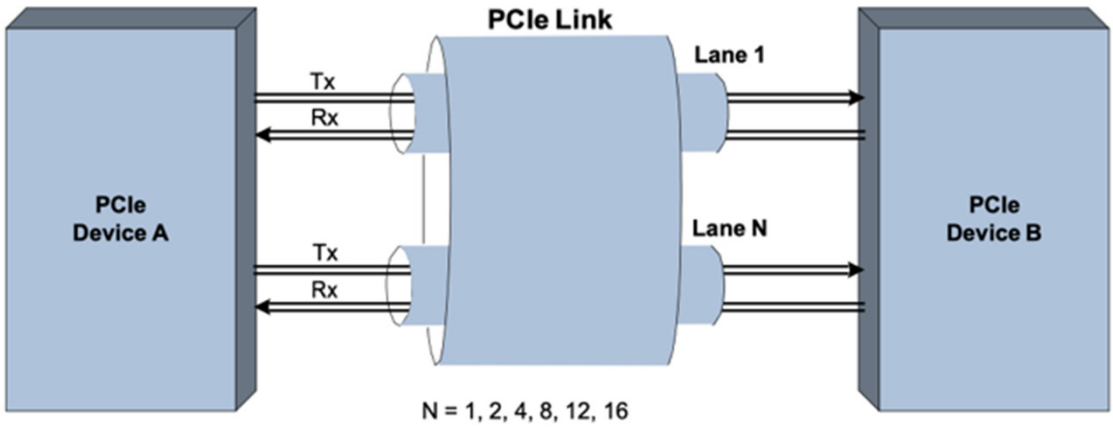

Figure 2: PCIe Link [3]

PCIe Generational Improvements

Every subsequent PCIe generation tends to double the previous generation's throughput. Although the Gen. 5.0 PCIe devices are just starting to make it to market, the PCIe Gen. 6.0 specification is slated for a 2021 release to meet market demands for applications such as machine learning and high-performance computing (Table 1).

Table 1: PCIe Generational Bandwidth Specifications [3][2]

	RAW BIT RATE (GT/S)	DATA THROUGHPUT PER LANE	MAX DATA THROUGHPUT (16 LANE DUPLEX)	YEAR RELEASED
PCIE 1.1	2.5 (8b/10b)	250 MB/s	8 GB/s	2003
PCIE 2.1	5.0 (8b/10b)	500 MB/s	16 GB/s	2007
PCIe 3.1	8.0 (120b/130b)	~ 1 GB/s	~ 32 GB/s	2010
PCIE 4.0	16.0 (120b/130b)	~ 2 GB/s	~ 64 GB/s	2017
PCIE 5.0	32 (120b/130b)	~ 4 GB/s	~ 128 GB/s	2019
PCIE 6.0	64.0 (PAM4 FLIT)	~ 8GB/s	~ 256GB/s	2021*

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The way PCI-SIG is approaching the new data rate requirement is by changing the encoding scheme from Non-Return to Zero (NRZ) to Pulse Amplitude Modulation with 4 levels (PAM4). The Bit Error Rate (BER) is expected to increase by several orders of magnitude by moving to PAM4, leading to the adoption of Forward Error Correction (FEC) for PCIe Gen. 6.0. Although the FEC is integrated into PCIe Gen. 6.0, the clock source specification is expected to require a 33% tighter rms phase jitter budget than the previous generation (Table 2).

Table 2: PCIe Gen. 4-6 Summary [5]

ARCH.	ELECT SPEC.	NOM ACCUR. (PPM)	SPR. SPCT (%)	TX/RX PLL BW, ORD, PEAKING MAX	CDR BW, ORDER, PEAKING	JITTER LIMIT* FOR (PS RMS @ RAW BER)		
						16GT/S (@10E-12)	32GT/S (@10E-12)	64GT/S (@10E-6)
Common Clock	4.0 v1.0	± 300	-0.5	2-4MHz 2nd, 01-2dB 2-5MHz 2nd, 01-1dB	10MHz 1st, 0dB	0.5	n/a	n/a
	5.0 v1.0	±100	-0.5	0.5-1.8MHz 2nd, .01-2dB	20MHz 1st 1.1MHz 1st 160kHz 1st	0.5	0.15	n/a
	6.0 v0.5	±100	-0.5	0.5-1.0MHz 2nd, 01-2dB	10MHz 1st 3.88MHz 1st 87kHz 1st	0.5	0.15	0.1
Sep. Ref. Indep. Spread	4.0 v1.0	±300	-0.5	2-4MHz 2nd, .01-2dB 2-5MHz 2nd, .01-1dB	10MHz 2nd, 1dB 400kHz 1st ~6MHz 400kHz	No spec (0.7/sqrt2)	n/a	n/a
	5.0 V1.0	±100	-0.3	0.5-1.8MHz 2nd, .01-2dB	20MHz 1st 1.1MHz 1st 160kHz 1st	No spec (0.7/ sqrt2)	No spec (0.25/ rt2)	n/a
	6.0 v0.5	±100	-0.3	0.5-1.0MHz 2nd, .01-2dB	20MHz 1st 1.1MHz 1st 160kHz 1st	No spec (0.7/ sqrt2)	No spec (0.25/ rt2)	No spec (0.13/ rt2)

*Simulation budgets are 0.7ps rms, 0.25ps rms, and 0.15ps rms for Gen. 4, 5, 6 respectively. Deterministic jitter induced by crosstalk is scaled by the filter only, not the BER multiplier.

Challenges Moving from PCIe 5.0 to 6.0

The biggest challenge adopting PAM4 is its effect on signal integrity. Forward error correction (FEC) has been implemented in the Gen. 6.0 spec. to combat this but at a cost. As a load/store architecture, there would be significant performance degradation for a few nanoseconds increase in latency, so PCI-SIG made it apparent that the FEC cannot afford to add more than a 2% latency hit over the Gen. 5.0 specification.

In an effort of achieving long-term compatibility and reliability, PCI-SIG is seeking to achieve an aggressive FIT score (Table 3). The FIT score has got to be far less than 1 and close to 0 for a x16 implementation. Because of this effort, every standard will be supported dating back to the 1.x release.

Table 3: PCIe 6.0 Requirements [2]

METRICS	REQUIREMENTS
Data Rate	64 GT/s, PAM4
Latency	<10ns adder for Transmitter + Receiver over 32.0 GT/s (including FEC)

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METRICS	REQUIREMENTS
Bandwidth Inefficiency	<2 % added over PCIe 5.0 across all payload sizes
Reliability	0 < FIT << 1 for a x16 (FIT - Failure in Time, number of failures in 109 hours)
Channel Reach	Similar to PCIe 5.0 specification under similar set up for Retimer(s) (maximum 2)
Power Efficiency	Better than PCIe 5.0 specification
Low Power	Similar entry / exit latency for L1 low-power state Addition of a new power state (LOp) to support scalable power consumption with bandwidth usage without interrupting traffic
Plug and Play	Fully backwards compatible with PCIe 1.x through PCIe 5.0
Others	HVM-ready, cost-effective, scalable to hundreds of Lanes in a platform

The Adoption of Pulse Amplitude Modulation

PAM4 modulation manifests three eyes and four levels (2 bits) to decode per clock cycle (Table 4). The move to PAM4 was dictated by difficulty of achieving a 32dB channel loss with NRZ encoding. Moving to PAM4 doubled the bandwidth without having to increase the sampling rate since the Nyquist frequency remains the same. In combination with the newly integrated forward error correction (FEC) requirement, the encoding scheme is to leverage gray encoding along with precoding to further reduce burst errors. Although these measures for error correction are being implemented, error correction will still be a challenge to pull off at a system level.

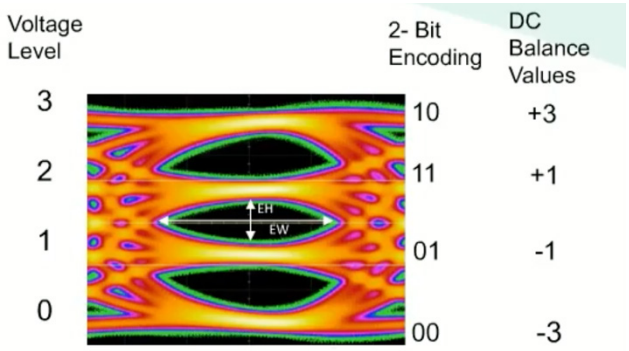

Figure 3: PCIe 6.0 Eye Measurement [2]

Table 4: PAM4 Thresholds [2]

ENCODING PER UNIT INTERVAL	TX VOLTAGE (V)	RX VOLTAGE (V)
00	-Vtx	V ≤ Vth1
01	-Vtx/3	Vth1 < V ≤ Vth2
10	+Vtx/3	Vth2 < V ≤ Vth3
11	+Vtx	V > Vth3

The reduced eye height and width are the culprits of errors not seen in the previous revisions of the specification (Figure 3). The main metric of focus is the First Bit Error Rate (FBER). It is the probability of

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the first error seen by the receiver. Just about any bit flip will propagate into a burst error. The secondary concern is the error correlation between lanes: When one lane manifests an error, it is likely that another lane will manifest an error as well.

The two ways to combat these errors are by implementing forward error correction (FEC) and cyclic redundancy checking (CRC). When an error propagates through a lane, the CRC is responsible for detecting the error. The error will then be passed through FEC in hopes that it will fix the error. If FEC does not resolve the error, then the error will trigger a link level retry. The addition of FEC in combination with CRC will consequently introduce a correction latency, which must stay below 2ns to sufficiently meet industry bandwidth expectations.

Clocking Architectures

There are three common architectures for PCIe. The most common architecture incorporated in modern PCIe designs is the Common Clock architecture (Figure 4). This architecture leverages a single clock source for all PCIe devices in the system. A common clock architecture is a great choice for systems that have multiple PCIe endpoints, but it can quickly run into clock skew limitations as the PCIe device count expands.

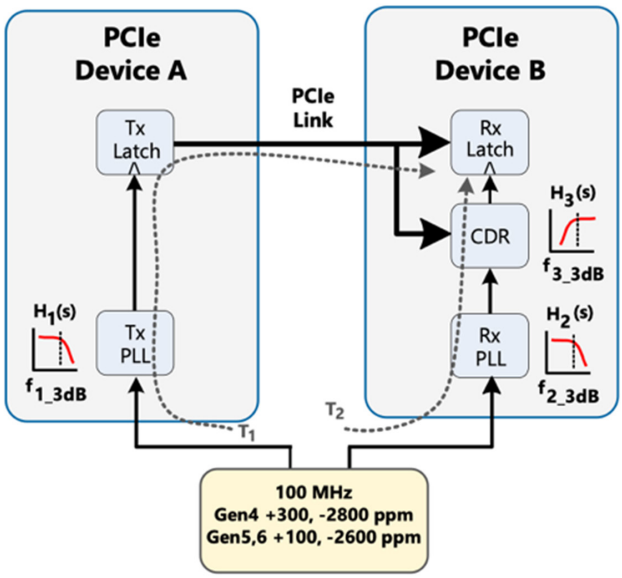

Figure 4: Common Clock Architecture [5]

The phase noise of the Common Clock architecture is calculated by taking the product of the clock source's rms phase noise against the system's transfer function (eq. 4). The system transfer function is found by multiplying the difference between Tx PLL (eq. 1) and Rx PLL (eq. 2) against the clock-data-recovery (CDR) transfer function (eq. 3).

$$\text{Tx PLL} \quad H_1(s) = \frac{2s\zeta_1\omega_{n1}+\omega_{n1}^2}{s^2+2s\zeta_1\omega_{n1}+\omega_{n1}^2} \qquad \textit{Equation 1}$$

$$\text{Rx PLL} \quad H_2(s) = \frac{2s\zeta_2\omega_{n2}+\omega_{n2}^2}{s^2+2s\zeta_2\omega_{n2}+\omega_{n2}^2} \qquad \textit{Equation 2}$$

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CDR $H_3(s) = \frac{s}{s+\omega_{n3}}$ *Equation 3*

Refclk Path Delay Difference: $T = |T1 - T2|$

Overall Transfer Function

$$H(s) = \left(H_1(s)e^{-st} - H_2(s)\right) H_3(s) \quad \textit{Equation 4}$$

$$H'^{(s)} = \left(H_2(s)e^{-st} - H_1(s)\right) H_3(s) \quad \textit{Equation 5}$$

Another approach is by separating clock sources. The Separate Clock architecture (SRIS) frees up the necessity of a sophisticated clock distribution scheme at the expense of increasing design complexity to stay compliant within the ±300ppm tolerance specification (Figure 5).

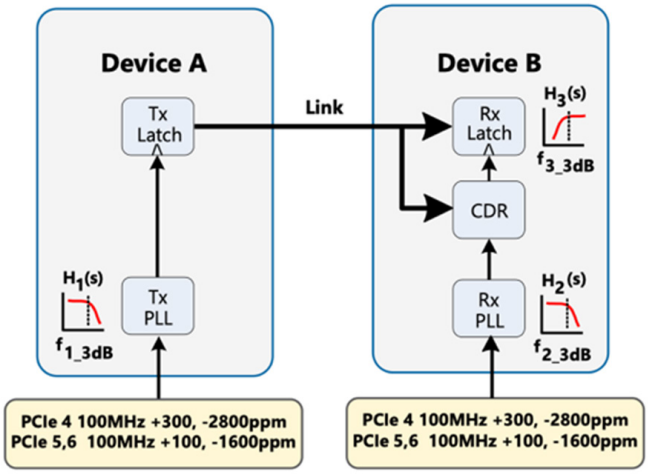

Figure 5: Separate Clock Architecture [5]

Similar to the Common Clock architecture, the clock source phase noise is bandpass filtered. With independent reference clocks, the phase noise can be found by taking the RSS (root sum square) of the Tx/Rx PLLs and CDR combined transfer functions (eq. 8). The system transfer function expresses the substantially tightened jitter requirements by choosing to split up clock sources.

$$H_1(s) = \frac{2s\zeta_1\omega_{n1}+\omega_{n1}^2}{s^2+2s\zeta_1\omega_{n1}+\omega_{n1}^2}$$

$$H_2(s) = \frac{2s\zeta_2\omega_{n2}+\omega_{n2}^2}{s^2+2s\zeta_2\omega_{n2}+\omega_{n2}^2}$$

$$H_{CDR}(s) = \frac{S^2}{s^2+sA+B} * \frac{S^2+2\zeta_2\omega_0 s+\omega_0^2}{S^2+2\zeta_1\,\omega_0 s+\omega_0^2} * \frac{s}{s+\omega_{n1}} \quad \textit{Equation 6}$$

$$h(s) = \frac{2s\zeta_2\omega_{n2}+\omega_{n2}^2}{s^2+2s\zeta_2\omega_{n2}+\omega_{n2}^2} \quad \textit{Equation 7}$$

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Since the reference clocks are independent of each other and their dominant jitter is random, their combined impact on the system should be root sum square of the individual terms (eq. 8).

$$X_{SRIS} = \sqrt{[X_1(s)H_1(s)H_{CDR}(s)]^2 + [X_2(s)H_2(s)H_{CDR}(s)]^2} \qquad \textit{Equation 8}$$

The simplest PCIe configuration is the Data Clocked architecture. The entire system depends on a single clock source from where the data is transmitted. This functionality is supported only in PCIe Gen. 2 and Gen. 3.

High-Speed Current Steering Logic

PCIe relies on High-Speed Current Steering Logic (HCSL) for its differential clocking. It is essentially a compromise between LVDS and LVPECL in respect to their power consumption and jitter tradeoffs. HCSL provides a high impedance output with quick switching speeds that maximizes common-mode noise rejection. The HCSL driver sources a continuous 14mA into 50Ω to ground on each trace (Figure 6). If properly terminated, each end (OUT+, OUT-) should see a 700mV swing.

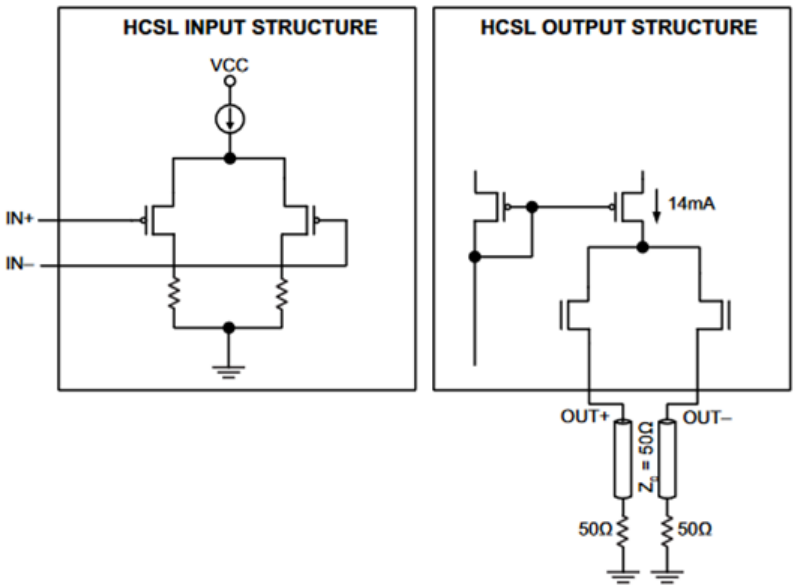

Figure 6: HCSL Input & Output Structure [4]

AX3 & AK2 Results and Discussion

Abracon's AX3 and AK2 ClearClock™ oscillators offer substantial improvement in phase noise performance, noticeable across all PCIe clocking architectures. This improved performance is the result of a proprietary design within the AX3 and AK2 family of ICs [6],[7]. The new design has a typical RMS phase jitter of less than 70fs over an integration bandwidth of 12kHz to 20MHz. The phase noise analysis of the AX3HAF1-100.000MHz as a reference is shown in Figure 7.

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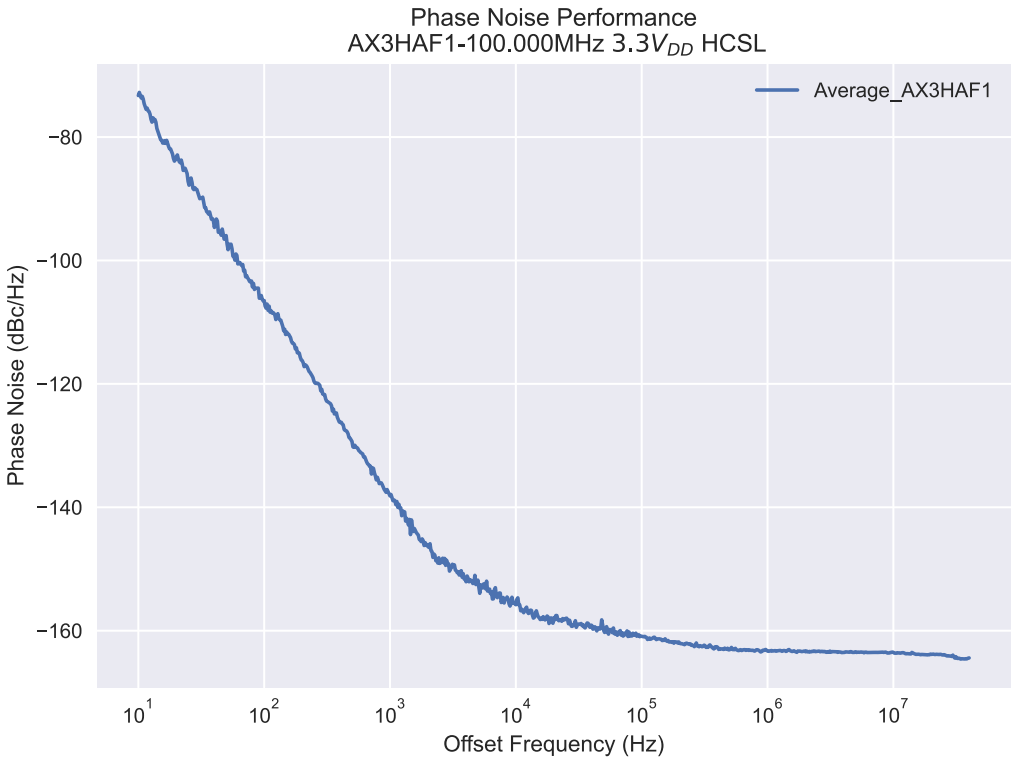

Figure 7: Average AX3HAF1-100.000MHz Phase Noise

For most applications, the 12kHz-20MHz integration bandwidth is sufficient, although PCIe 6.0 demands a larger bandwidth of 10kHz-50MHz and only specifies the phase noise seen at the Rx latch.

PCI-SIG recommends adding three folds to each phase noise measurement generated by the signal source analyzer (Figure 8). Each fold is a noise floor extension across one Nyquist band (100MHz/2).

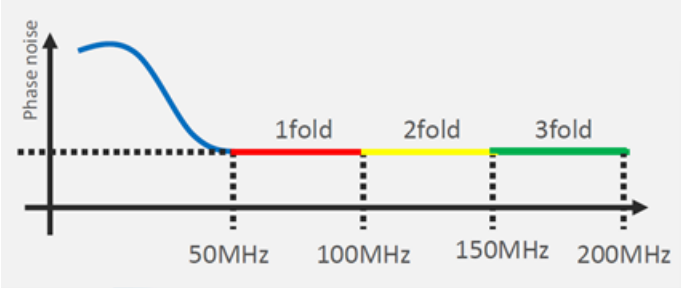

Figure 8: Noise folding Correction [5]

The phase noise seen by the Rx latch can be calculated after the noise folding correction has been applied. The transfer functions are then applied from the previously mentioned filter stages before the Rx latch. The filter constants are conveniently provided by Silicon Labs and can be applied using the Silicon Labs PCIe Clock Jitter Tool [5].

A filter compliance report was generated on the average of five Abracon AX3HAF1-100.000MHz phase noise measurements, and the results have been consolidated in Table 5.

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Table 5: AX3HAF1-100.000MHz Compliance Summary

CLASS	DATA RATE	ARCHITECTURE	SPEC	SPEC HF RMS	SPEC LF RMS	MAX HF RMS	MAX LF RMS
GEN1	2.5 Gb/s	Common Clock	1.1 2.1 3.1	-	-	**155.45 fs**	16.43 fs
GEN2	5 Gb/s	Common Clock	1.1 2.1 3.1	**3.1 ps**	3 ps	**134.56 fs**	8.19 fs
GEN3	8 Gb/s	Common Clock	3.1 4.0	**1 ps**	-	**46.42 fs**	1.98 fs
GEN4	16 Gb/s	Common Clock	4.0	**500 fs**	-	**46.42 fs**	1.98 fs
GEN5	32 Gb/s	Common Clock	5.0	**150 fs**	-	**18.35 fs**	0.80 fs
GEN6	64 Gb/s	Common Clock	6.0	**100 fs**	-	**11.12 fs**	0.36 fs
GEN6	64 Gb/s	Separate Clock SRNS	6.0	**106 fs**	-	**10.31 fs**	0.52 fs
GEN6	64 Gb/s	Separate Clock SRIS	6.0	**106 fs**	-	**10.31 fs**	0.00 s

The primary metric to focus on is the High Frequency RMS jitter being the integration bandwidth of 10kHz to 50MHz. To adequately measure the phase noise for SRIS and SRNS architectures, the root sum square of the jitter from two separate clocks is needed. The approximate combined HF rms jitter of the AX3HAF1-100.000MHz is 14.58fs, calculated using equation 8. This exceeds the 106fs maximum requirement needed for the typical PCIe 6.0 SRNS and SRIS architecture. It can be deduced from the table above that the capability of the AX3HAF1-100.000MHz, and the rest of the 100MHz AX3 and AK2 series, easily exceeds the reference clock jitter requirements for PCIe 6.0 and all previous revisions of the specification.

Conclusion

PCI Express is one of the most popular interconnects on the market today, and the demand for it is substantially growing year over year. The PCI Express standard shall see increased market adoption because of its reliability, long-term generational hardware support, power efficiency, and cost effectiveness. As each generational improvement is made, the link layer is the primary culprit to upstream issues.

Abracon's AX3 and AK2 3rd overtone offerings take on these generational improvements with ease. Specifically, for the PCIe 6.0 requirement, the clock source must have an intrinsic rms jitter performance of 100fs maximum over the 10kHz to 50MHz integrated bandwidth. Abracon's ClearClock™ family of devices meets and exceeds this threshold in various package sizes by 7-fold with typical PCIe clocking architectures.

For customers seeking miniature form-factor solutions, Abracon's AK2 and AX3 in 2.5x2.0mm and 3.2x2.5mm SMD packages, respectively, are ideal for space-constrained designs that require exceptional rms jitter performance for the future of high-speed communication protocols such as PCI Express. Along with the enhanced phase noise performance, the ClearClock™ family offers a stringent, all-inclusive frequency accuracy over a 20-year product lifetime.

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