ABRACON®

APPLICATION NOTE 1025

18pF Crystals May Not Oscillate with Energy Saving MCUs

The 18pF plated Quartz Crystals may no longer be the ideal choice for a typical clocking circuit using an off-the- shelf MCU. As silicon geometries have shrunk over the last decade, the Pierce oscillator loop embedded in typical MCU's has also evolved.

The latest 22nm, 14nm and now 10nm silicon geometries are bringing many benefits such as decrease in total IC size & reduction in power consumption – while incorporating feature rich capabilities. However, these advancements present challenges in the typical Pierce oscillator loop for system engineers.

In particular, these advancements in silicon geometry have decreased amplifier/inverter's transconductance, gm , in the crystal oscillator loop. The results are power starved oscillation circuits that are marginally functional. These circuits run the risk of failing to startup due to total capacitive loading, changes in temperature & bias levels, etc.

The sustainability of oscillations can be quantified with the following ratio:

$$GainMargin = \frac{g_m}{4*ESR*(2\pi F)^2*(C_0 + C_L)^2} \quad .....(1)$$

Ideally, for robust oscillations in a real-world environment, the goal is this ratio to be greater than five.

The equivalent series resistance ESR and the plating load CL of the quartz crystal have a profound impact on the closed-loop gain margin. Additionally, package capacitance (inclusive of electrode's capacitive impact) is another variable that affects the overall oscillation sustainability. It is evident from equation (1) that as the gm decreases, it is imperative to simultaneously reduce ESR, CL and CO.

Older crystals with higher plating loads such as 18pF are not capable of competing with the higher gain margins offered by the latest generation of crystals with lower plating loads. In addition, these older crystals will eventually be incapable of starting up in low power applications. This is not the first time for a plating load to become obsolete. Due to similar reasons, the industry has seen the disappearance of the 32pF plated crystal.

Calculating the Gain Margin is difficult due to the lack of information in MCU datasheets and inability to anticipate board-to- board parasitics. For these reasons, designers have increasingly utilized Abracon's Pierce Analyzer Service (PAS) to determine their crystal oscillator in-circuit performance.

The PAS was used to observe the behavior of Abracon's highest and lowest plating loads for ABM10 and ABM10W series (3.2x2.5mm package). To remain consistent, all measurements utilized Renesas's RL78 MCU. Current through the crystal was measured with crystals plated at 4, 6, 10 and 18pF and data was interpolated for 8, 12, 14 and 16pF. Additionally, the gain margin was calculated by inserting a series resistor with the crystal and its value was increased until the oscillations ceased. Figure (1) outlines the relationship between gain margin and current through the crystal at various plating loads.

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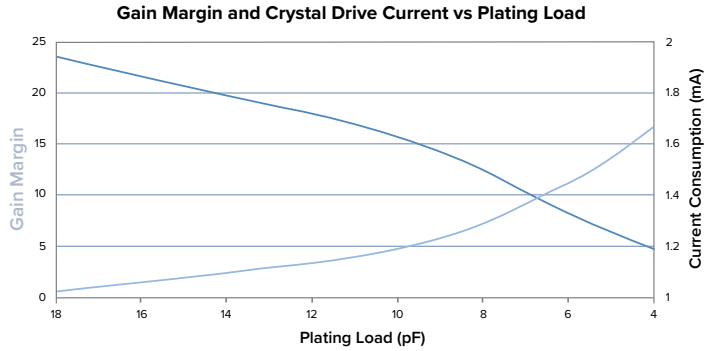

Figure 1

Crystal Series	Max ESR (Ω)	Plating Load (pF)	Crystal Operating Drive Current (mA)	Reduction in Crystal Operating Drive Current	Gain Margin	Operationally Reliable
AMB10W	80	4	1.19	39%	16.57	YES
ABM10W	80	6	1.33	31%	11.23	YES
AMB10	80	10	1.63	16%	4.78	Marginal
ABM10	80	18	1.94	Baseline	0.66	NO

Based on these measurements, a designer can achieve superior performance by utilizing lower plating load, IoT optimized quartz crystals from Abracon. The gain margin increased from < 1.00 to > 15 using MAXIMUM ESR of 80 ohms which provides the worst case scenario for these crystals at 16.00MHz carrier. It is widely accepted that the gain margin needs to be greater than (5) for robust oscillations, when accounting for board parasitics, part-to- part variation, operating temperature range and other unforeseen problems that could cause oscillation to cease.

It should be pointed out that using crystals with lower plating loads, even with the same maximum ESR specification, lowers the total current through the crystal. This also helps in long term viability of the crystals, as they are being driven with less power – while yielding optimal closed loop gain margin. In our next installment we will examine the effect of crystal susceptibility to phase/frequency balancing capacitors at lower plating loads.

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5/18