ABRACON®

APPLICATION NOTE 1024

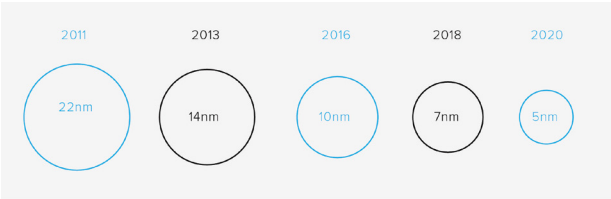
IoT, Wearable, & Low Power: Performance Optimized Quartz Crystals

The IoT market is on an explosive pace of growth with industry projections of $470 billion for IoT related hardware, software, and other comprehensive solutions. The current installed base of 15.4 billion devices is expected to exceed 30.7 billion by 2020.

Major IC OEM's including Intel, ARM, Samsung and QUALCOMM are actively engaged in the development of reduced process geometries down to 10nm and even 7nm FinFET architectures.

Major Foundry Semiconductor Fabrication Trends

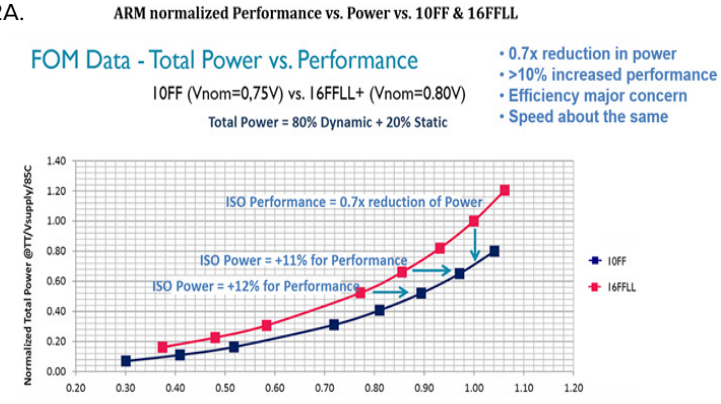
1A.



Intel	10nm production expected by mid 2017, 7nm by 2018/19
TSMC	10nm started production in 2016, 7nm by 2018
Samsung	10nm production started in Q4-2016, 7nm in R&D
ARM	Working with TSMC for 10nm, 7nm in R&D

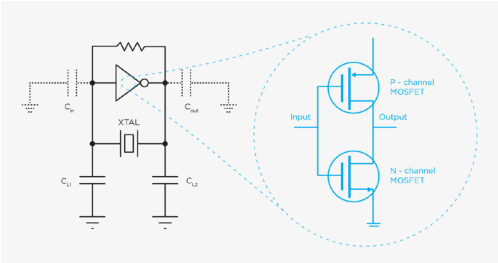
The primary driving force behind this industry trend is related to the reduction in total consumed power, while improving overall performance. This effort is being undertaken to facilitate the practical implementation of battery powered end-solutions (consumer, medical, IoT, industrial, etc.), requiring extremely low power in a feature-rich environment. These advancements, however, have significantly impacted the traditional clocking circuit.

2A.

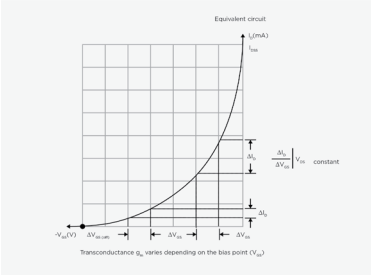


The integrated clocking scheme is predominantly based on the world renowned Pierce Oscillator configuration; a simplified configuration is depicted in graphic 3A-3B.

3A.



3B.



As the low power operation becomes paramount, the current mirrors biasing the inverter amplifier stage in the Pierce Oscillator loop are "starving" the amplifier. This approach has a significant impact on the transconductance of the inverter amplifier block which, in-turn, has a profound effect on the forward gain margin (G_M) of the closed-loop oscillator circuit.

The relationship between the forward gain (G_M) and amplifier transconductance is defined as follows:

$$G_M = g_m / g_{mcritical} \quad \text{.....} \quad (1)$$

Whereas;

g_m = inverter amplifier's transconductance in µA/V

$g_{m(critical)}$ = critical transconductance value to keep the amplifier in linear region

For robust oscillations using an inverter amplifier as the gain stage, it has been a well-established industry practice to target $G_M \geq 5.0$ with a minimum desired value of ≥ 3.0.

For closed loop oscillator circuit, $g_{m(critical)}$ is defined as follows:

$$g_{m(critical)} = 4 * ESR * (2\pi F)^2 * (C0 + CL)^2 \quad \text{.....} \quad (2)$$

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Whereas;

ESR = Effective Series Resistance of the resonator element (generally a quartz crystal)... units in kΩ's or Ω's.

F = Resonant frequency of the resonator element (in the case of quartz crystals, generally parallel resonant frequency @ a specific plating load)... units in kHz or MHz

C_0 = Composite package and electrode capacitance of the resonator element..... units in pF.

C_L = Plating load of the resonator element..... units in pF.

From equation (1), to achieve higher G_M value, it is best to decrease the $g_{m(critical)}$ value. From equation (2), with the final goal of increasing the G_M value, it is critical to reduce the impact of all three parameters (ESR, C_0 and C_L).

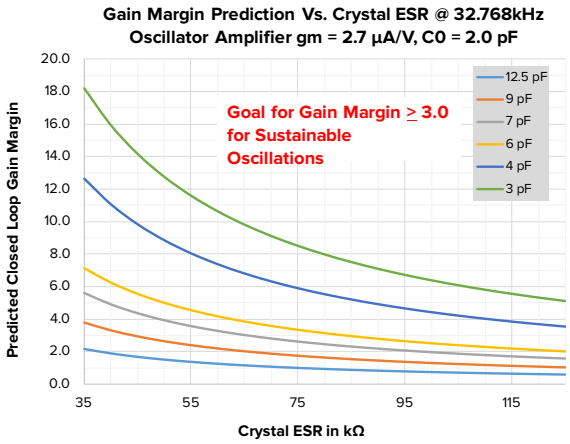
The value of C_0 can be well controlled with careful design of the electrode pattern, as well as, utilization of state-of-the-art, small profile, ceramic packages. The ESR and C_L however, present a unique challenge. These two parameters have a diverging dependence meaning that, as C_L is decreased, ESR tends to rise so the net impact has a tendency to stay flat or worsen.

This challenge is further exacerbated with significantly reduced values of the intrinsic g_m within the latest geometry FPGAs, µControllers, µProcessors, ASSP, etc. For example, 14nm node based, low-energy µControllers have specified g_m value of as low as 2.7µA/V for the 32.768kHz embedded oscillator loop.

Let's illustrate the impact on the closed loop gain margin (G_M) with varying plating loads at fixed g_m and C_0 value in a 32.768kHz oscillator loop, over an ESR variance for the tuning fork, 32.768kHz crystal.

As is evident from this analysis, the crystal plating load has a profound impact on the closed-loop-gain-margin (G_M); with fixed C_0 and g_m values. Further, as the g_m value decreases in 10nm and smaller geometry silicon, the ability to sustain oscillations will become increasingly challenging.

4A.



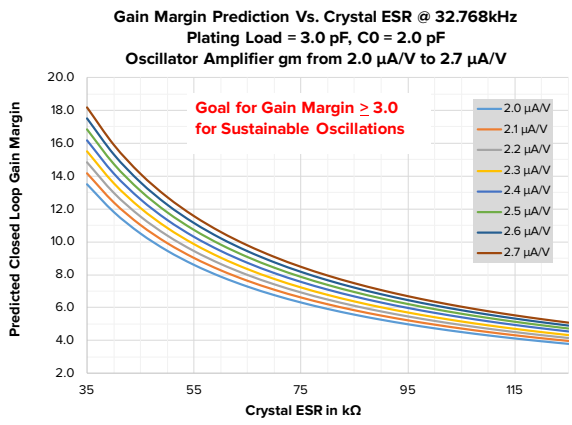
It is also important to point out that the inverter amplifier's g_m will generally have a spread of ±5% to >±15% from part-to-part and wafer-to-wafer. Therefore, it is essential that the crystal resonator design accommodates real-world tolerance effects.

Abracon has taken above specified variables into account in developing its ABS06W and ABS07W series of tuning fork crystals in 2.0x1.2x0.6 mm and 3.2x1.5x0.9 mm, respectively.

To achieve optimal in-circuit performance, Abracon optimized the electrode pattern to reduce the overall effects of C_0 such that, the maximum guaranteed (electrode + package) capacitance is 2.0 pF in 2.0x1.2x0.6mm package and an industry leading 1.30 pF maximum in 3.2x1.5x0.9 mm package.

With revolutionary blank design and processing techniques, Abracon was able to substantially reduce the ESR of these solutions over extended operating temperature range of -40°C to +125°C; while simultaneously reducing the plating load to Industry leading 3.0 pF.

5A.



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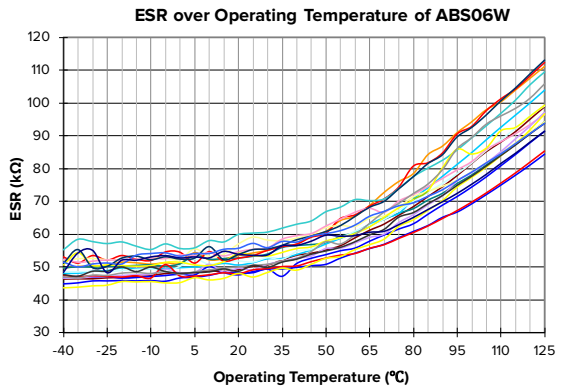
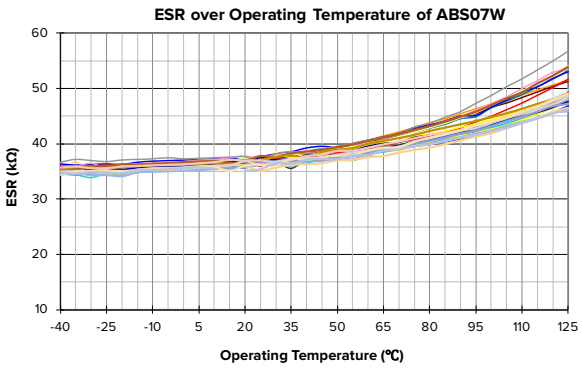
5B.

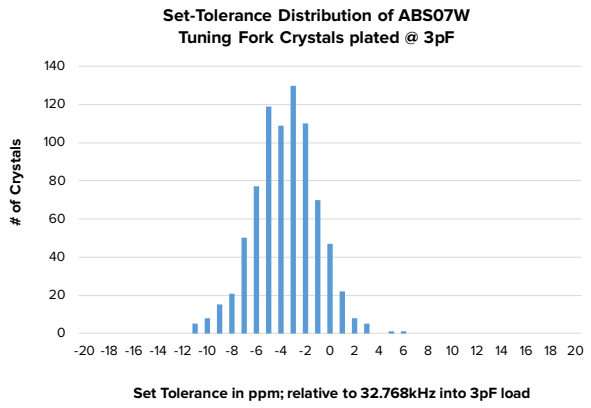


5C.

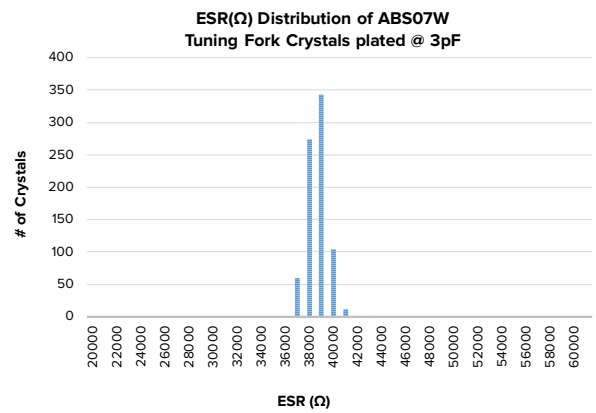


Abracon has employed unique production tuning techniques to tighten both the set-tolerance and ESR distribution at room temperature.

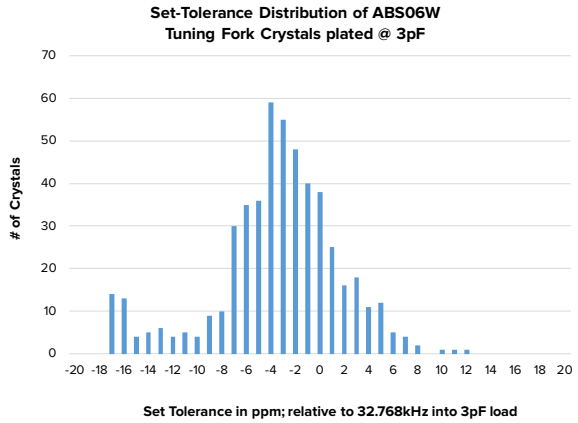
6A.



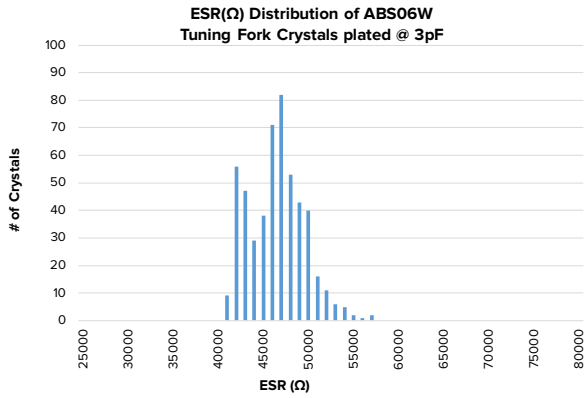
6B.



6C.



6D.



Plots 6A through 6D depict Abracon's ability to minimize the ESR value of these solutions; while reducing the plating load to an industry leading 3.0 pF.

It should be noted that the majority of the consumer market/IoT end-solutions have an operating temperature range of -20°C to +70°C. In this narrower operational range, ABS06W & ABS07W devices offer exceptionally low ESR values; further enhancing the in-circuit gain margin with today's energy saving silicon. Abracon has taken measures to ensure state-of-the-art ESR performance over the entire -40°C to +125°C operational range and is the only OEM that guarantees ESR performance values over wider operational temperature ranges.

Abracon also recognized the need to employ these design, process, and production techniques and successfully implemented them to offer a broad breadth of IoT optimized quartz crystals in the MHz range. Since one package cannot satisfy all end-solution form-factor needs, Abracon has developed the following solutions addressing a comprehensive market need:

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7A.

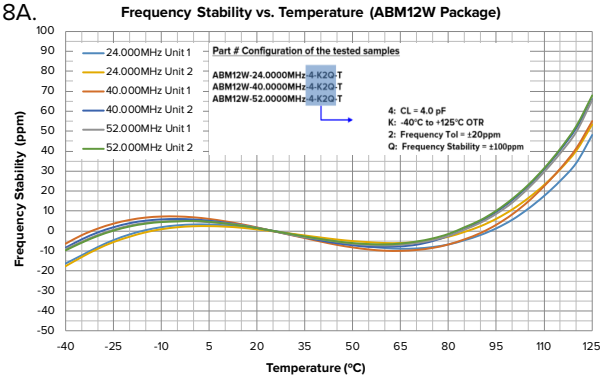
Series Name	Size (mm)	Frequency Range (MHz)	CL Options (pF)	ESR Range (Ω)	Available OTR (°C)
ABM12W	1.6x1.2x0.4	24 to 52	4, 6, 7 & 8	80 to 120	-40 to +125
ABM11W	2.0x1.6x0.5	16 to 50	4, 6, 7 & 8	60 to 200	-40 to +125
ABM10W	2.5x2.0x0.6	16 to 50	4, 6, 7 & 8	70 to 100	-40 to +125
ABM8W	3.2x2.5x0.75	10 to 54	4, 6, 7 & 8	50 to 150	-40 to +125
ABS07W	3.2x1.5x0.9	32.768kHz	3	45-70	-40~+125
ABS06W	2.0x1.2x0.6	32.768kHz	3	65-120	-40 ~+125

Abracon's ability to plate these solutions at industry leading 4.0 pF plating capacitance, while keeping the ESR at the minimum possible value ensures that these solutions not only mate well with today's 22nm or 14nm FinFET technology, but more importantly, are optimized to ensure optimal performance with next generation solutions including 5nm nodes in the near future.

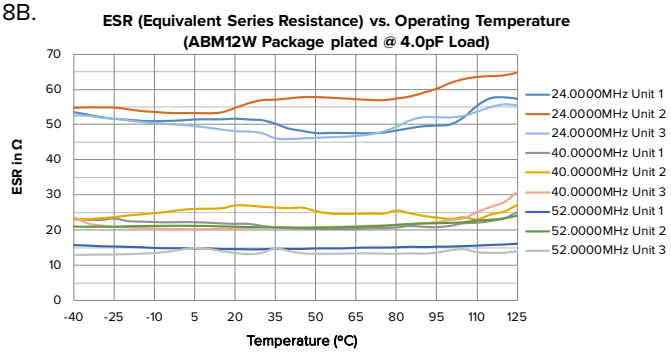
The data in plots 8A through 8H outline the superior performance of Abracon's MHz, IoT Optimized Quartz Crystals plated at 4.0 pF load:

ABM12W package: (1.60 x 1.20 x 0.40 mm)

8A.

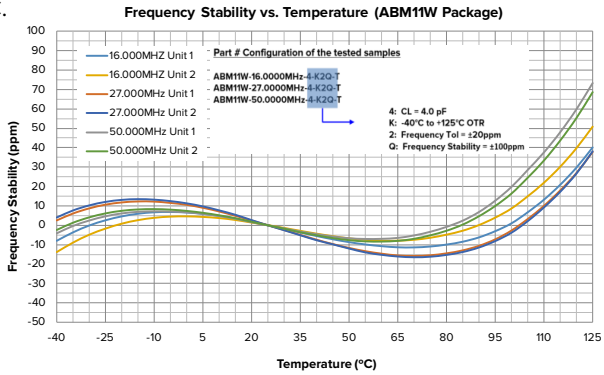


8B.

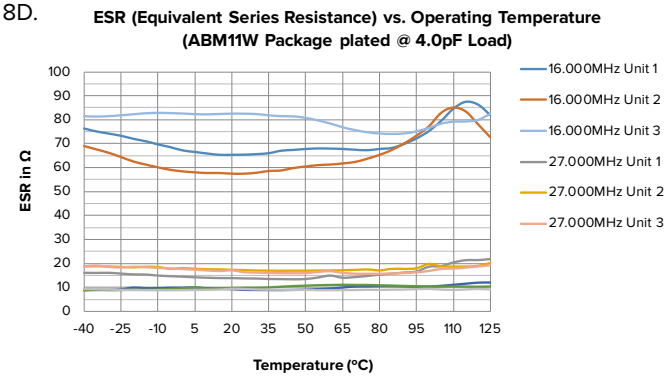


ABM11W package: (2.00 x 1.60 x 0.50 mm)

8C.

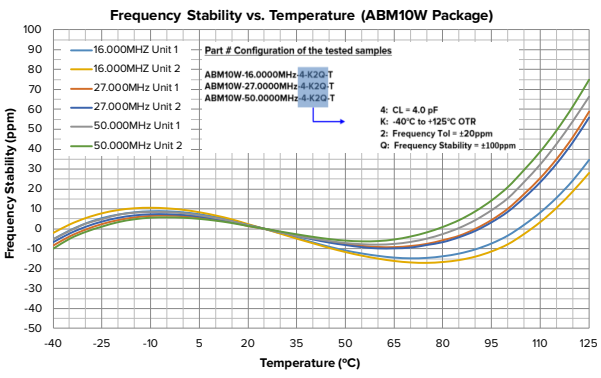


8D.

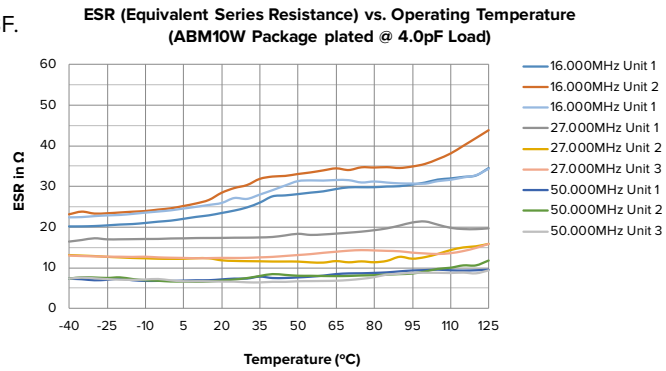


ABM10W package: (2.50 x 2.00 x 0.60 mm)

8E.



8F.



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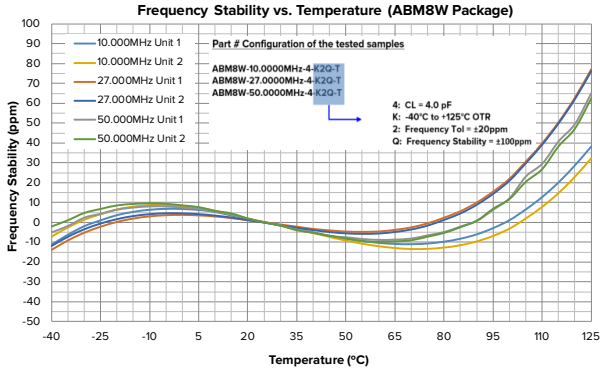
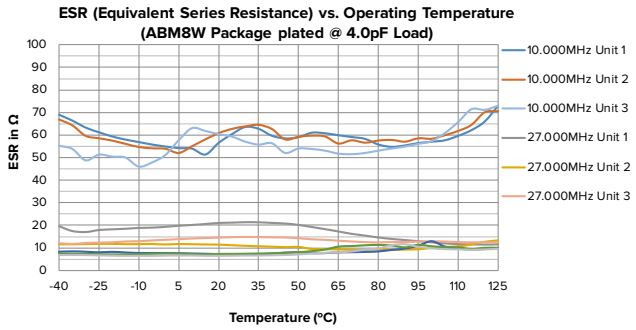
ABM8W package: (3.20 x 2.50 x 0.70 mm)

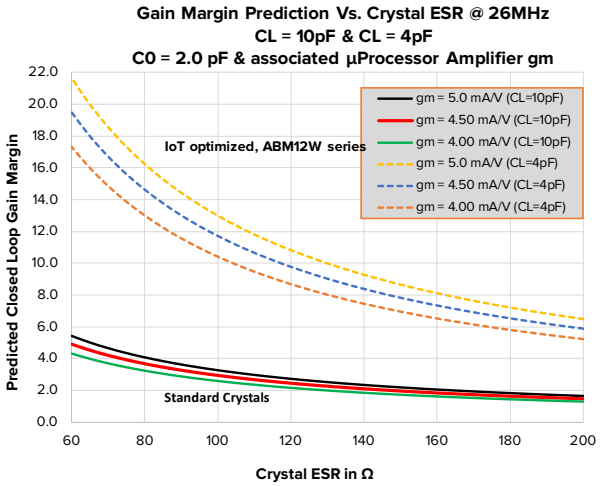
8G.



8H.



9A.



Abracon's IoT Optimized Quartz Crystals are in stock.

Abracon's ability to:

- guarantee (electrode + package capacitance) "C0" of 2.0pF maximum
- accurately plate the Quartz Blanks @ 4.0 pF plating load, in as small as 1.6x1.2x0.4 mm package
- and simultaneously reduce the ESR of the crystal

collectively represents a paradigm shift in the performance capability of optimized quartz crystals at commodity prices.

This capability yields a significant enhancement in the closed loop Gain Margin (G_M) with exiting 22nm or 14nm nodes and, ensures a robust performance with next generation 10nm, 7nm and even 5nm FinFET silicon. A comparison below between crystals plated at 4.0 pF vs. 10.0 pF with C0=2pF clearly outlines this advantage.

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ENGINEERING SERVICES

DID IT PAS?™

Abracon provides an advanced proprietary Pierce analyzer test service (PAS) that validates quartz crystal performance and long term operation in-circuit. The ability to sustain oscillation for a given quartz crystal oscillator design depends heavily on the crystal's motional parameters, board parasitics and oscillator circuit characteristics. The oscillator circuit is a closed loop system that sustains oscillation at an operating frequency depending on the crystal parameters including, crystal plating capacitance (CL), crystal equivalent series resistance (ESR), external loading capacitors, trace parasitics and the oscillator amplifier's gain & phase response. The PAS test service provides a direct measurement of all variables associated with the quartz crystal oscillation. With all variables taken into account, Abracon is able to provide an optimized solution and detailed report that includes:

- Motional parameters (Cm, Lm, ESR, Co)
  - Motional parameters
  - Narrow band frequency response plot
  - Wide band frequency response plot
  - Admittance versus susceptance plot
  - Frequency dependence versus load capacitance plot
- Circuit design margin calculation
- Recommendations for achieving optimal operating point

Orderable Part Number	Lead Time
PAS-BC1WK	1 Week
PAS-BC2WK	2 Week
PAS-BC3WK	3 Week

ANTENNA OPTIMIZATION SERVICES

Abracon offers in-system tuning services for patch and chip antennas. By characterizing the antenna performance in the end system or product, this service takes the guess work out of RF verification while offering corrective measures that re-tune the system for center frequency and impedance mismatch. This provides maximum system efficiency delivering many benefits including, extended RF range, improved sensitivity and can reduce the required power consumption for a given level of transmit range.

This service is offered for the APAE and APA series of passive patch antennas covering a variety of RF bands from few MHz to thousands of MHz for applications, such as RFID, GPS/GLONASS, LPWA, WiFi, ISM radios, and Iridium. Patch antennas are compact with excellent coupling gain and are easy to use. However, frequency shifts may occur due to the layout, proximity to other components and the design of the ground plane. If de-tuned center frequency is discovered during testing, the patch antenna design can be fine-tuned for the particular device environment. These adjustments match the layout for maximum gain at the center frequency of the application.

This service also applies to the ACAG, ACAJ and AMCA series of chip antennas. Chip antennas such as the ACAG0201-2450-T with 2.0x1.25mm footprint are ultra-compact with good gain that increases sensitivity for applications, such as Bluetooth, Bluetooth Low Energy (BLE), WiFi/WLAN, and Zigbee. These chip antennas require a matching network that optimizes antenna impedance thereby improving the efficiency. The input impedance is matched using lumped elements like inductors and capacitors for the center resonant frequency of the antenna. Higher efficiency guarantees more radiated power and increased range for antennas.

The test requires a fully functional system to be shipped to Abracon and typically takes 4 weeks to complete. **Orderable Part Number: ABAOS-5WK**

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