


HF/UHF SMD VCTCXO

 ESD Sensitive 25.78 x 22.48 x 7.37 mm
Datasheet #0710E

Features

- Ultra High Frequency -up to 1GHz
- Small, Low profile SMD Package
- Very Low Phase Jitter and Phase Noise
- Excellent Frequency Stability
- CMOS, Sine-wave, Differential PECL or LVDS outputs available
- Stratum 3 available

Applications

- COTS/Dual use

Absolute Maximum Ratings

Parameters	Symbol	Condition	Min	Typ	Max	Unit	Notes
Input Break Down Voltage	V _{cc}		-0.5		5.5	V	
Storage Temperature	T _s		-40		105	°C	
Control Voltage	V _c		-1		9	V	

Electrical

Parameters	Symbol	Condition	Min	Typ	Max	Unit	Notes
Frequency Range	F	CMOS Sine-wave PECL, LVDS	30 30 30		200 1,000 1,000	MHz	
Input Voltage	V _{cc}	Code 0 Code A	4.75 3.135	5.0 3.3	5.25 3.465	V	
Input Current	I _{cc}	CMOS, Sine PECL, Sine, LVDS			30 100	mA	@100MHz, 3.3V @622MHz, 3.3V
Frequency Stability	ΔF/F	Overall, available			±4.6		20 years
Frequency Stability	ΔF/F	vs Temperature vs V _{cc} Aging		±0.5 ±0.1 ±1 ±3.5	±1	ppm ppm/V ppm/year ppm	See chart First Year 10 Years
Calibration	ΔF/F	As shipped, 25°C		±0.5	±1	ppm	
Load		CMOS Sinewave PECL LVDS	15pf/10KOhm Internally AC-coupled 50 Ohm 50 Ohm to V _{cc} -2V or Thevenin equivalent 100 Ohm between the outputs, receiving end				
Duty Cycle		At 50%	45/55	50/50	55/45	%	CMOS, PECL, LVDS
Rise/Fall Time	Tr/Tf	20 to 80%		3 0.35		ns	CMOS PECL, LVDS
Logic "1" level	V _{oh}	CMOS	0.9V _{cc}			V	
Logic "0" level	V _{ol}	CMOS			0.1V _{cc}	V	
Logic "1" level	V _{oh}	PECL	V _{cc} -0.96		V _{cc} -0.81	V	100K available
Logic "0" level	V _{ol}	PECL	V _{cc} -1.85		V _{cc} -1.65	V	100K available
Output levels LVDS	V _{od}	Differential amplitude	247	330	454	mV	
		Amplitude error			50	mV	
	V _{of}	Offset Voltage	1.125	1.25	1.375	V	
		Offset Voltage error			50	mV	



Electrical (cont.)

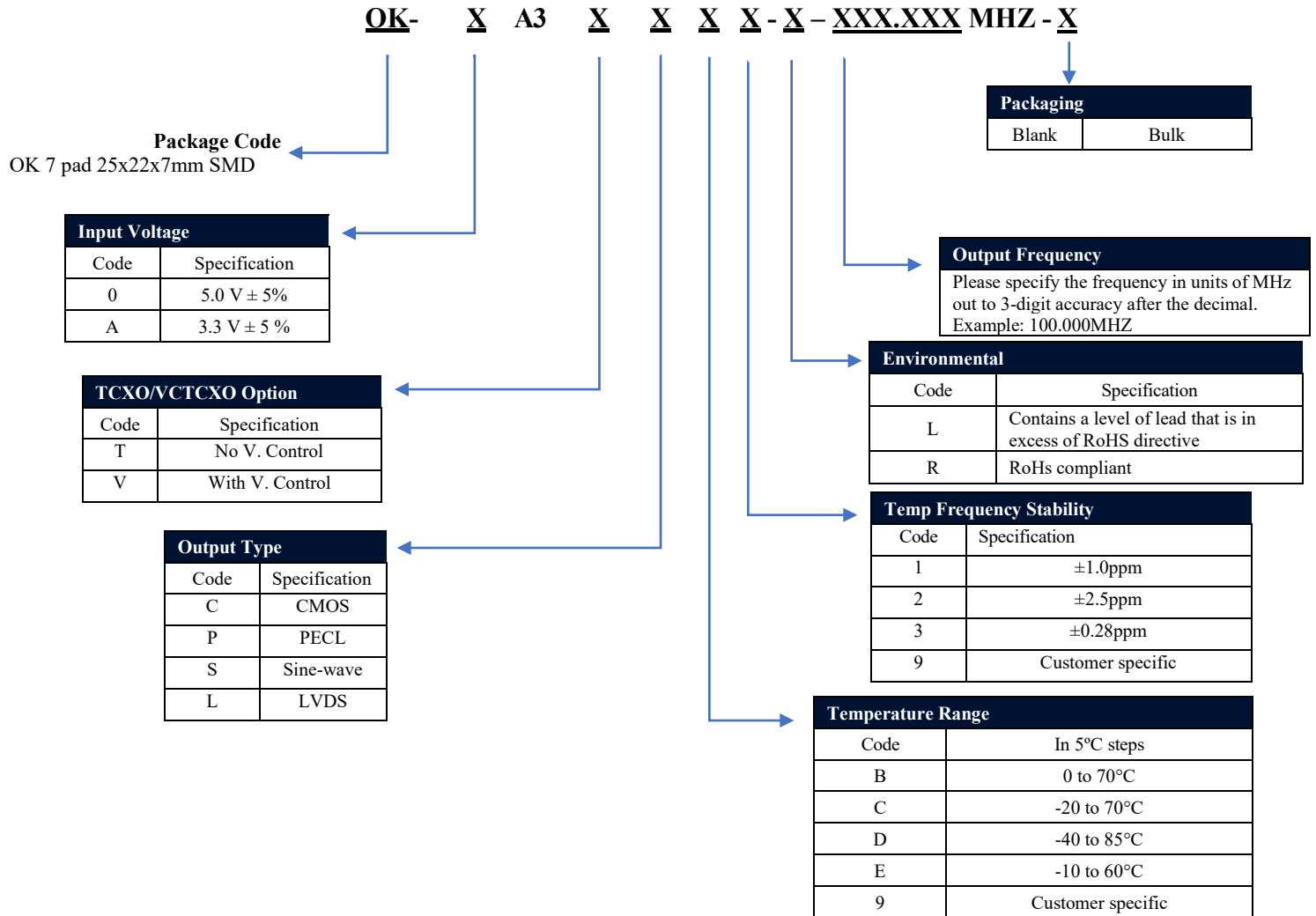
Parameters	Symbol	Condition	Min	Typ	Max	Unit	Notes
Output Power	P	Sinewave Into 50 Ohm $\leq 400\text{MHz}$	0 4	3 7		dBm	3.3V 5.0V
		Sinewave into 50 Ohm >400MHz	-5 0	0 5	5		3.3V 5.0V
Start up Time	Ts			2	10	ms	
Phase jitter		1 sigma		0.4 0.2	1 0.4	ps	100Hz to 20MHz 12kHz to 20MHz
Sub-harmonics		PECL, LVDS, Sine CMOS, Sine		-45	-40 none	dBc	F>250MHz F<250MHz
Spurious					-60	dBc	
Harmonics		Sine-wave		-30	-25	dBc	
SSB Phase Noise		@10Hz		-80		dBc/Hz	@100MHz
		@100Hz		-110			
		@1KHz		-140			
		@10KHz		-155			
		@100KHz		-160			
SSB Phase Noise		@10Hz		-60/-60		dBc/Hz	@622MHz; PECL, LVDS/Sine
		@100Hz		-90/-90			
		@1KHz		-120/-120			
		@10KHz		-140/-145			
		@100KHz		-145/-150			
Input Impedance			>10 KOhm				
Control Voltage	Vc		0		3.3	V	For 3.3V supply
			0		5.0	V	For 5.0V supply
Modulation Bandwidth	MB		2Hz				Contact Factory for wider MB
Deviation		Vc=0V to 3.3V, 25°C	±5	±7		ppm	

Environmental and Mechanical

Parameter	Description
Operating temp. range	0°C to 70°C, -40°C to 85°C, see chart page 1
Mechanical Shock	Per MIL-STD-202, Method 213, Cond. E
Thermal Shock	Per MIL-STD-883, Method 1011, Cond. A
Vibration	Per MIL-STD-883, Method 2007, Cond. A
Hermetic Seal	Leak rate less than 1×10^{-8} atm.cc/s of helium (crystal only)
Soldering conditions	See MAX reflow profile below; The device may be reflowed once. Reflowing upside down is not allowed. NO CLEAN assembly is recommended



Creating a Part Number



Not all combinations are available. Consult Factory.

Temperature Code Table

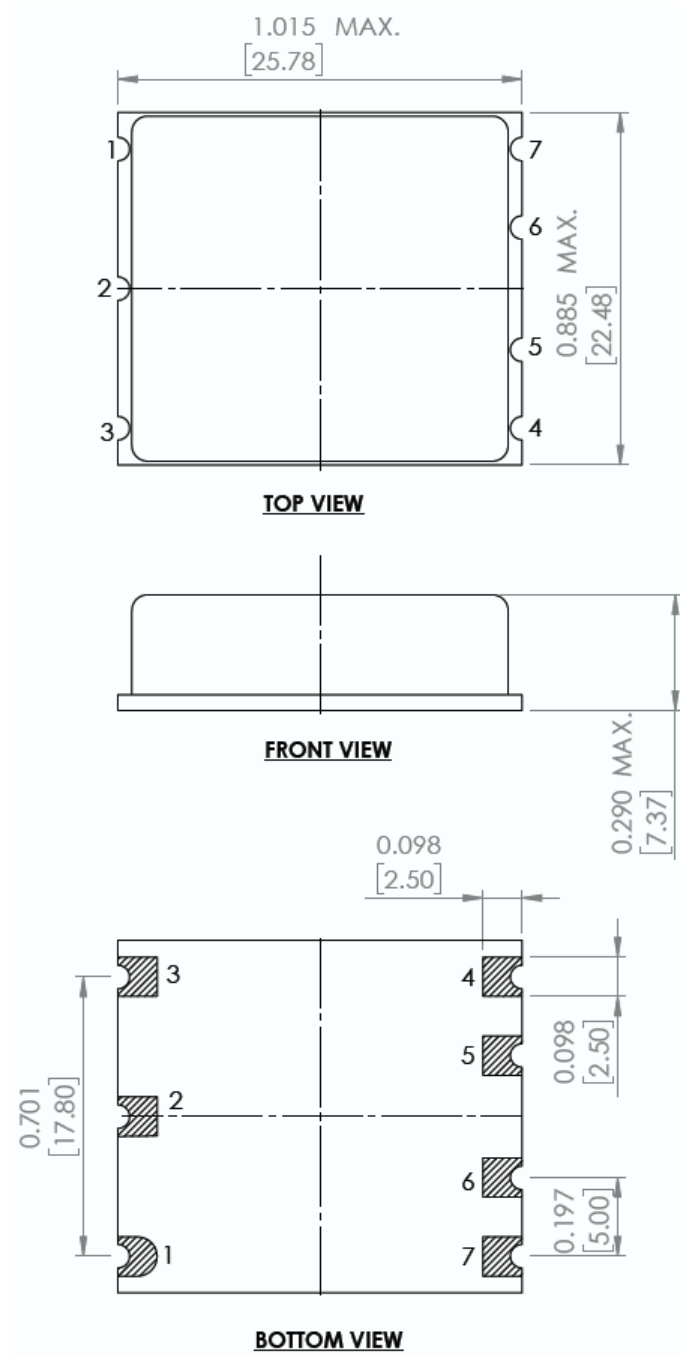
Letter	Temp °C	Letter	Temp °C	Letter	Temp °C	Letter	Temp °C	Letter	Temp °C	Letter	Temp °C
A	-40	F	-15	K	10	P	35	U	60	Z	85
B	-35	G	-10	L	15	Q	40	V	65		
C	-30	H	-5	M	20	R	45	W	70		
D	-25	I	0	N	25	S	50	X	75		
E	-20	J	5	O	30	T	55	Y	80		

Notes:

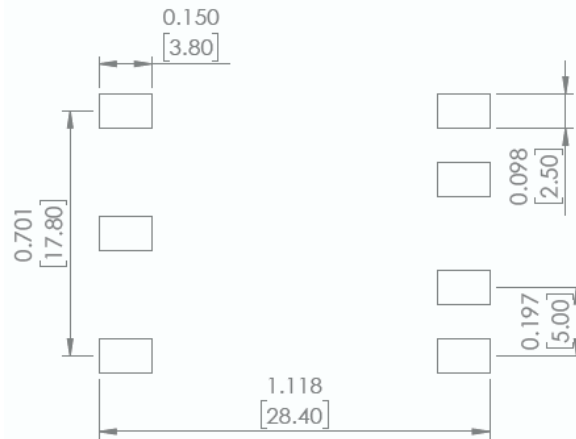
1) All parameters, unless otherwise specified, are at nominal conditions, ie: T= 25°C, Nominal Vcc & Nominal Load



Mechanical Dimensions



Recommended Land Pattern



OUTLINE TOLERANCE:

±0.015 [0.40] (UNLESS OTHERWISE SPECIFIED)

Note: For frequency stability over temperature ±1 ppm and tighter, the package height may be 10mm or 12.5mm.

Pin #	Function
1	Voltage Control
2	NC
3	Vcc
4	Output, CMOS or Sine
5	Output, PECL/LVDS
6	Comp. Output, PECL/LVDS
7	GND

Dimensions: inches [mm]



Reflow Profile [JEDEC J-STD-020]

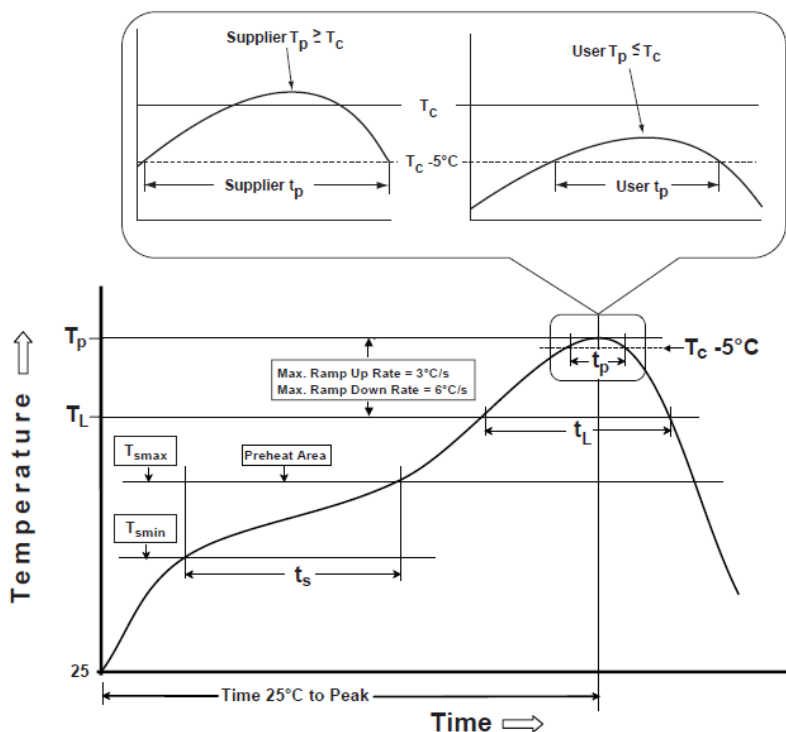


Table 1

SnPb Eutectic Process Classification Temperatures (T_c)		
Package Thickness	Volume mm^3 <350	Volume mm^3 \geq 350
<2.5 mm	235°C	220°C
\geq 2.5 mm	220°C	220°C

Table 2

Pb-Free Process Classification Temperatures (T_c)			
Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm - 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat / soak		
Temperature minimum (T_{smin})	100°C	150°C
Temperature maximum (T_{smax})	150°C	200°C
Time (T_{smin} to T_{smax}) (t_s)	60 - 120 sec.	60 - 120 sec.
Average ramp-up rate (T_{smax} to T_p)	3°C/sec. max	3°C/sec. max
Liquidous temperature (T_L)	183°C	217°C
Time at liquidous (t_L)	60 - 150 sec.	60 - 150 sec.
Peak package body temperature (T_p)*	see Table 1	see Table 2
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20 sec.	30 sec.
Ramp-down rate (T_p to T_{smax})	6°C/sec. max	6°C/sec. max
Time 25°C to peak temperature	6 min. max	8 min. max
Reflow cycles	1 max	1 max

*Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

**Tolerance for time at peak profile temperature (t_p) is defined as supplier minimum and a user maximum.